ALICE FoCal-E PAD 検出器の信号読み出しに向けたVMM2 チップの性能評価

Examining the SRS VMM2 based hybrid as a front-end board for the ALICE FoCal-E Pad detector

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3/19/16
Introduction
ALICE FoCal-E upgrade project at forward region (LHC long shutdown in 2020)

FoCal-E (Electro-magnetic calorimeter)

HGL (High Granularity Layer)
- Shower position measurement
- MAPS technology
  (pixel 25 \( \mu \)m)
- Utrecht university (Nederland)

LGL (Low Granularity Layer)
- Photon shower energy measurement
- Silicon PAD technology
- Oak Ridge National Laboratory (U.S)
  & University of Tsukuba
Current readout electronics system for FoCaI-E Pad

FoCaI-E
Analog signal from each LGL to Summing board

APV25
Pre-amplifier, shaper, etc..

SRS
ADC (Analog Digital Converter) + FEC (Front End Concentrator)
Analog signal Convert to Digital signal response to computer

mmDAQ
Data taking and monitoring
Current problems of FoCAL-E pad and possible solution

1) Energy measurement is saturated near at 50GeV beam energy. To meet our physics goal need more energy dynamic range up to 300GeV.

2) Data taking rate with APV25 is 1kHz. Need faster data taking rate around 1MHz at forward region.

New readout system with VMM2 hybrid is tested with RD51 group.
New readout system with VMM
VMM2 hybrid
• Standard Panasonic connector (130 pin)
• 2 x VMM2 ASICs
• 1 x Spartan FPGA + 1 Flash
• 128 channel (64 x 2)
• readout rate could be 5 MHz.
- VMM can get analog signal through shaper
- VMM has ADC (Analog Digital Converter) inside the chip
  => This function makes digital signal output
  => It could be faster readout system compared to APV25 based SRS system with shorted ADC process
- VMM has internal test pulse
Readout system of VMM2 hybrid

- **VMM2**
  - Discriminator, shaper,
  - ADC (Analog Digital Converter), etc..

- **SRS**
  - D-CARD + FEC (Front End Concentrator)
  - Readout digital signal
  - Response to computer

- **NTU Athens (BNL)**
  - Control VMM2 chips and take data

**VMM2 hybrid**

**SRS**

- HDMI

- **PC**
  - NTU Athens

- Ethernet
Analysis software
NTU Athens software – connect and control VMM2
Gain
It can select lots of gain as 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC

It could take wider energy dynamic range

Peak time
It can select rise time of signal 25, 50, 100, 200 ns

Monitoring channel
You can select channel From 1 to 64 channel
Results
Response check by internal Test Pulse DAC with oscilloscope

100 DAC  
200 DAC  
300 DAC

Pdo (peak detector output)  
= return value of Amplitude  

Tdo (time detector output)  
= return value of Rise time
Linearity check with internal test pulse by gain variation

Low gain

High gain

Pdo vs Test pulse DAC value
Gain dependence
(0.5, 1.0, 3.0, 4.5, 6.0, 9.0, 12 16)

Gain 1.0 - 9.0 shows linearity.
VMM test with Micro Megas
Gas electric field

VMM2 hybrid
VMM2 Response check With Micro Megas detector

Trigger

Analog signal by VMM

Micromesh signal
Summary & outlook
Summary

• Development & Research of new readout for FoCAI - E pad

• Built a test bench for VMM2 hybrid at RD51 lab

• Checked VMM2 hybrid response with internal, external pulse

• Tested VMM2 hybrid with Micro Megas detector

Outlook

• Development new software for test higher speed readout.

• VMM3 (next version of VMM2) will be produced and tested as a new readout system.

• New LGL summing board toward VMM will be developed.

• Beam test will be conducted for FoCAI-E with VMM hybrid.
Back up
ALICE Upgrade Project – FoCal detector (toward LHC long shutdown at 2020 years)

- **location of installation**
  - 7m at z direction from collision point.

- **acceptance**
  - $3.3 < \eta < 5.3$

- **structure**
  - electro-magnetic calorimeter (FoCal-E)
  - hadron calorimeter (FoCal-H)

- **purpose**
  - To Detect jet effect and direct photon at forward.

$\eta = 5.3$
$\eta = 3.3$
$Z = 7 \text{ m}$
Sending internal analog signal within VMM2

For IP Connection
(ping status 10.0.0.2)

Start acquisition

Gain, Peak time, Monitoring Channel, etc..

Control internal test pusler DAC

Start to make root file

Decide root name and directory

Close to make root file

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3/19/16
64 channels

Can be controlled

SP=adjustable polarity
SC=Sensor Capacitance
SL=Leakage Current disable
ST=1.2pF, Test Capacitor enable
SM=Mask enable

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**Addc Depreciated**
Calibration => It can make macros with internal test pulse.
  Gain、Pulse range、channels、Number of Events

Trigger Data => to observe response of VMM2 with external trigger
You can check the analog signal before Analog Digital Conversion With oscilloscope
アナログ信号のピークの大きさ

信号の大きな変換に対して小さく反応する
Low Gain

信号の小さな変換に対して大きく反応する
High Gain

Gainの大きさ毎に、DACの大きさとアナログ信号のピークの大きさの依存性が確認できた

・High Gainでは弱い信号(Low Energy)の読み出し
・Low Gainでは強い信号(High Energy)の読み出しが期待される

Gain = 0.5mV/fC
Gain = 1.0mV/fC
Gain = 3.0mV/fC
Gain = 4.5mV/fC
Gain = 6.0mV/fC
Gain = 9.0mV/fC
Gain = 12 mV/fC
Gain = 16 mv/fC

Peak time = 200ns

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RD51 Collaborationの紹介
Development of Micro-Pattern Gas Detectors Technologies

・Micro Pattern Gas Detectors技術的発展とその応用を目指す。

・その技術の基礎と応用された研究に向けて必要とされるelectronic-readout systemの開発も行なっている。

・APV25, VMM prototypeを開発した。
Some bugs of VMM
しかし、VMM2 prototypeチップにはバグがある。

バグはどこからくるのか？

reason1) Cross talk　　reason2) bit flipping　 reason3) 原因が分からないバグ
Reason 1) Cross talk (high gain and high Test Pulse DAC)

21チャンネルのみにアナログ信号を送った結果、違うチャンネルのでも反応をしていることが確認できた。

Channel & Entry number

Entries: 156707
Mean: 12.03
RMS: 9.381
2) Bit flipping

Meanデータの倍数に信号が来るように見える現象があった。
reason3) chip is bad.

Cross talkとBit flippingの現象以外にも原因が分からない

結果が見えた。この結果もprototypeのバグとして考えられる。
Check VMM2 Thermal data.

I tested thermal result of VMM2

With agilent u1251b.
This Ceramic has lots of small holes.
VMM2チップの温度が上がり、チップに損害を与える可能性があったため、温度低下のため、Ceramicを用いたVMM2チップの温度調節

70℃→60℃

時間 Vs 温度

Just connecting VMM2 to FEC

Running VMM2

Just connecting VMM2 to FEC

Running VMM2

時間

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SRS System card

・D-CARD
  <= VMM2から送られて来たデジタル信号をFEC boardに送る。
  <= VMM2に電力を提供する。
  (VMM2の消費電力はAPV25の3倍)

・FEC V6
  <= D-CARDからのデータを処理し、PCへデータを送る。

電源モジュールを搭載したmini crateなどをまとめたシステムのことであるDCARD

FEC V6
Analog response with internal pulser

Δx = 68 ns
Δy = 60 mV

Δx = 73 ns
Δy = 80 mV

Δx = 86 ns
Δy = 88 mV

Δx = 92 ns
Δy = 90 mV
Δx = 64ns, Δy = 80mV

Δx = 96ns, Δy = 94mV

Δx = 160ns, Δy = 97mV

Δx = 208ns, Δy = 97mV

Gain 3.0 mV/fC, Test pulser DAC 400
All channel test

128 ch pin + 2 GND pin

(130pin panasonic connector)
Data taking Condition

Data trigger length 200ns
delay time 0s
trigger rate 2000Hz

結果

・各チャンネル毎にPdo値が違う
・GNDの方にも一緒に信号を送って結果、データに揺らぎが生じた

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Data taking condition

gain -> 9mV/fC, peak time -> 200ns
data, trigger pulse length -> 200ns
delay time -> 0s
from 100Hz to 3000Hz

Trigger rate vs entry number

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External Signal test

Function Generator
External trigger & external signal

VMM2
Discriminator, shaper, Peak & Time detector, ADC (Analog Digital Converter)

SRS
D-CARD + FEC (Front End Concentrator)

NTU Athens
Data taking & monitoring
One channel test
Channel 58

Peak time 200ns