ALICE FoCal-E PAD 検出器の信号読み出しに向けたVMM2 チップの性能評価

Examining the SRS VMM2 based hybrid as a front-end board for the ALICE FoCal-E Pad detector

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Introduction

ALICE FoCAl-E upgrade project at forward region(LHC long shutdown in 2020)

FoCal-E (Electro-magnetic calorimeter)

HGL(High Granularity Layer)

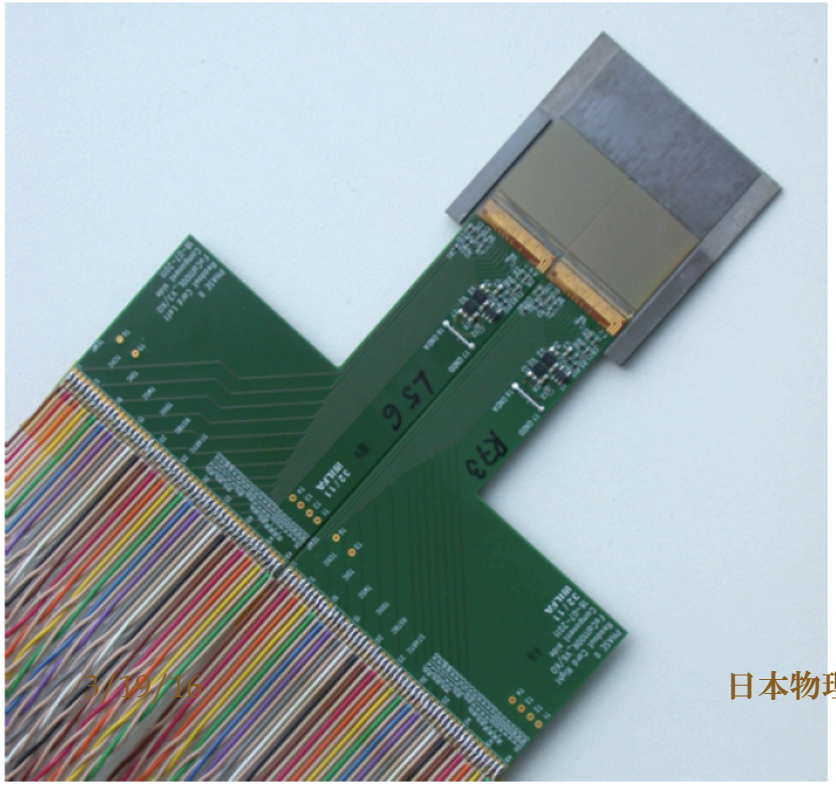
Shower position measurement
MAPS technology
(pixel 25 μ m)

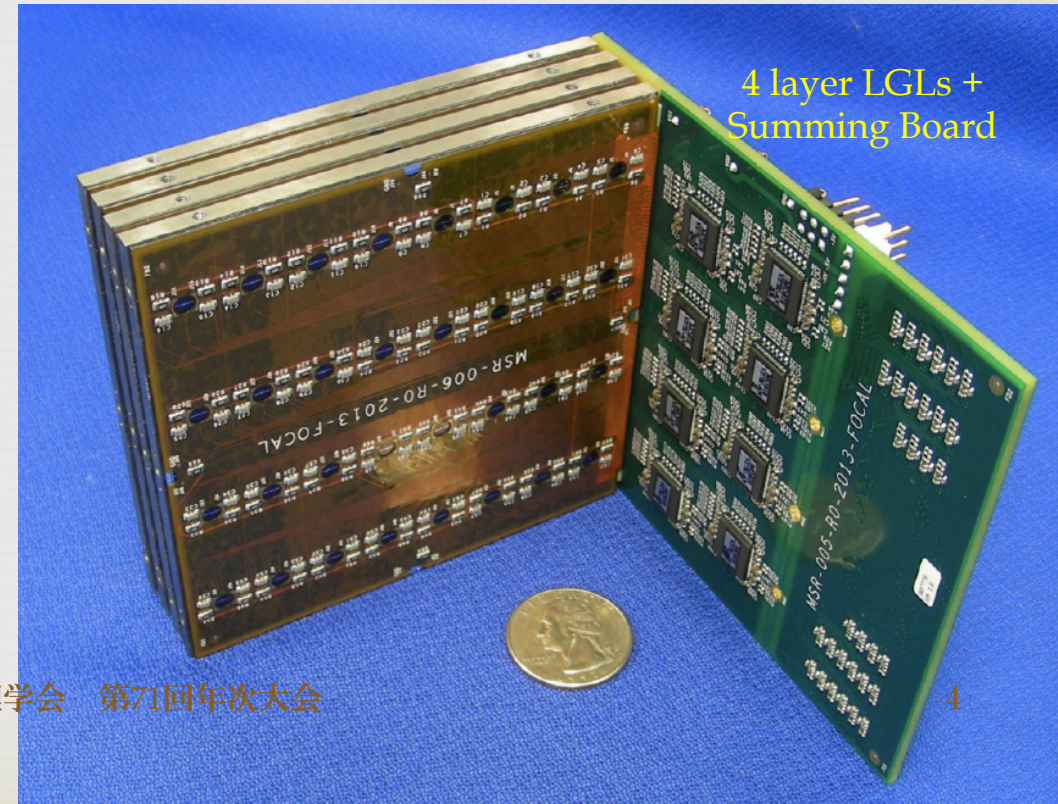
Utrecht university(Nederland)

LGL(Low Granularity Layer)

Photon shower energy measurement
Silicon PAD technology

Oak Ridge National Laboratory(U.S)
& University of Tsukuba





Current readout electronics system for FoCAl-E Pad

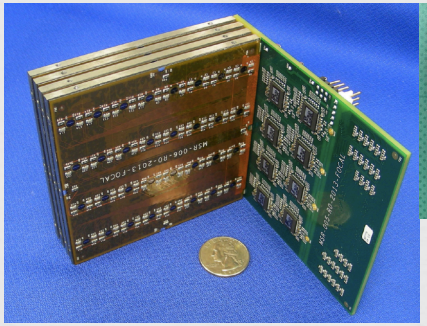
FoCAl-E
Analog signal from each **LGL** to Summing board

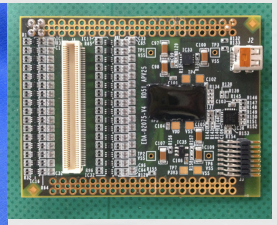
APV25
Pre-amplifier, shaper, etc..

SRS
ADC(Analog Digital Converter)
+FEC(Front End Concentrator)
Analog signal Convert to Digital signal response to computer

mmDAQ
Data taking and monitoring

FoCal-E → APV25



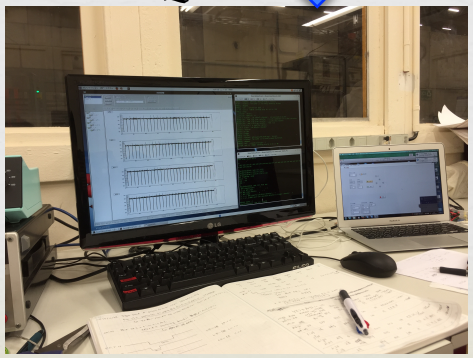


HDMI

SRS

PC
mmDAQ

Ethernet



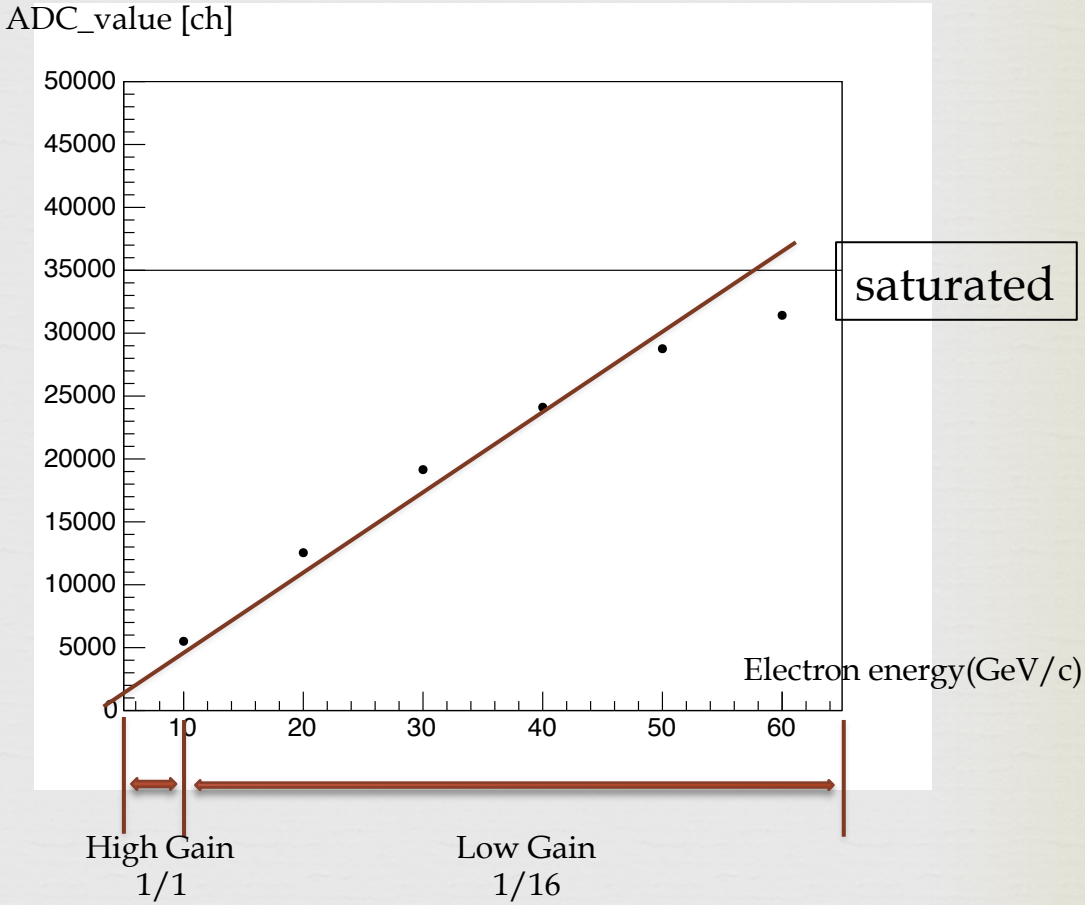
Current problems of FoCAl-E pad and possible solution

1) Energy measurement is saturated near at 50GeV beam energy

To meet our physics goal need more energy dynamic range up to 300GeV

2) Data taking rate with APV25 is 1kHz.

need faster data taking rate around 1MHz at forward region.

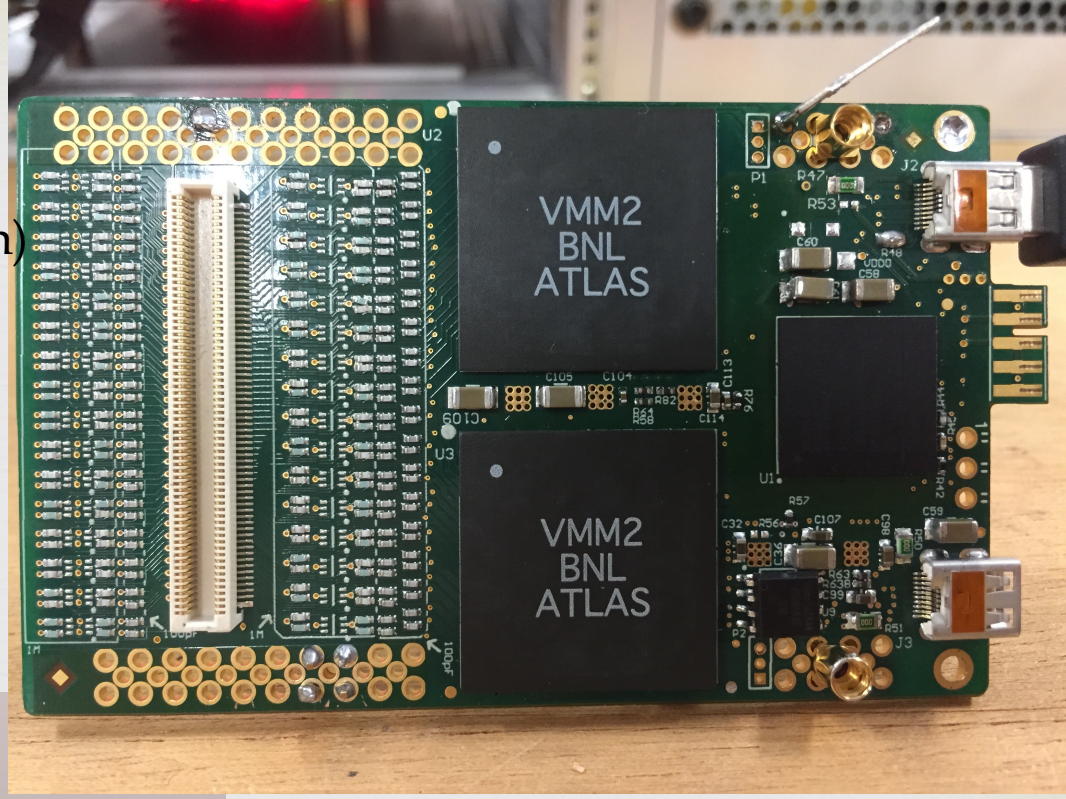


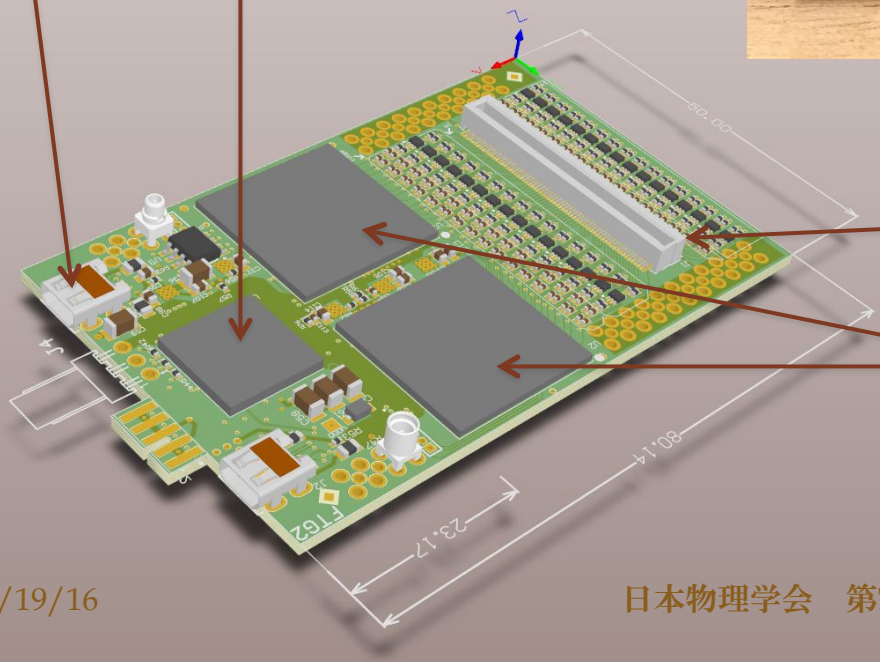
New readout system with VMM2 hybrid is tested with RD51 group.

New readout system with VMM

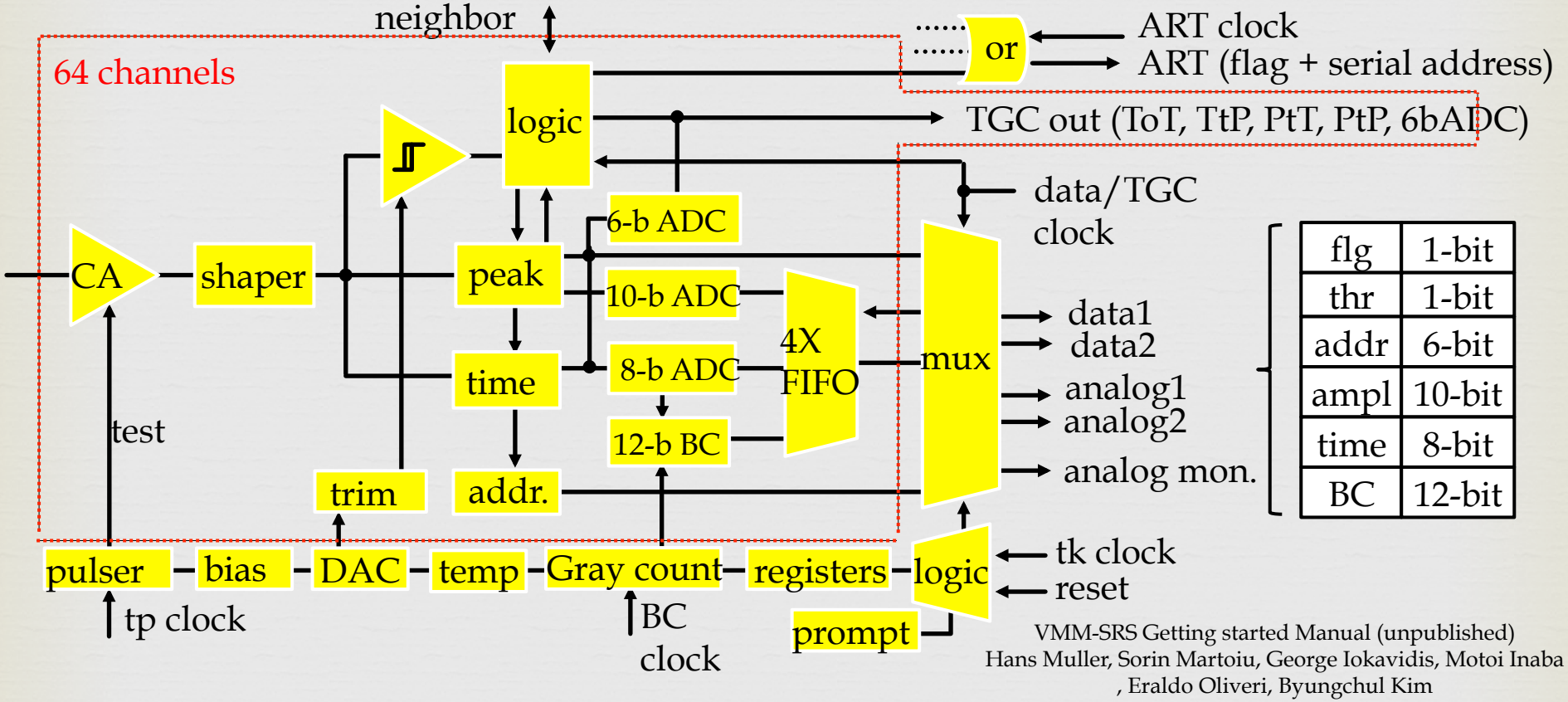
VMM2 hybrid

- Standard Panasonic connector(130pin)
- 2 x VMM2 ASICs
- 1 x Spartan FPGA + 1 Flash
- 128 channel (64 x 2)
- readout rate could be 5MHz.





VMM2 Architecture - Complete ASIC



VMM-SRS Getting started Manual (unpublished)
Hans Muller, Sorin Martoiu, George Iokavidis, Motoi Inaba , Eraldo Oliveri, Byungchul Kim

- VMM can get analog signal through shaper
- VMM has ADC(Analog Digital Converter) inside the chip
  - =>This function makes digital signal out put
  - =>It could be faster readout system compare to APV25 based SRS system with shorted ADC process
- VMM has internal test pulse

Readout system of VMM2 hybrid

VMM2
Discriminator, shaper,
ADC(Analog Digital Converter),etc..

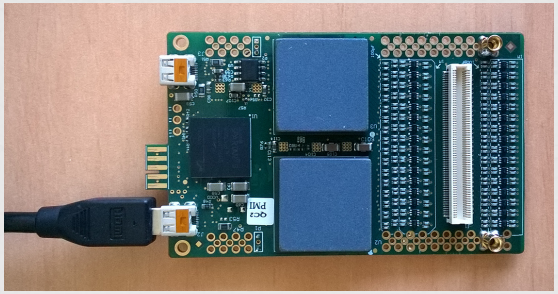
SRS

D-CARD
+FEC(Front End Concentrator)

Readout digital signal
Response to computer

NTU Athens(BNL)
Control VMM2 chips and take data

VMM2 hybrid

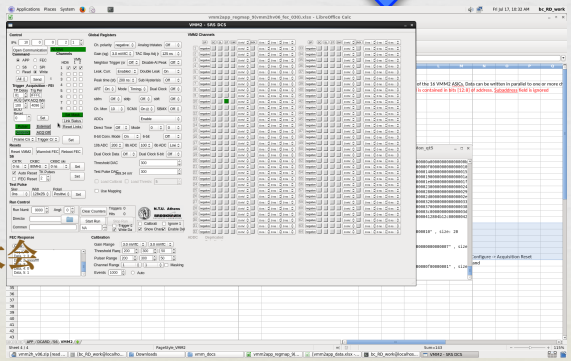


HDMI

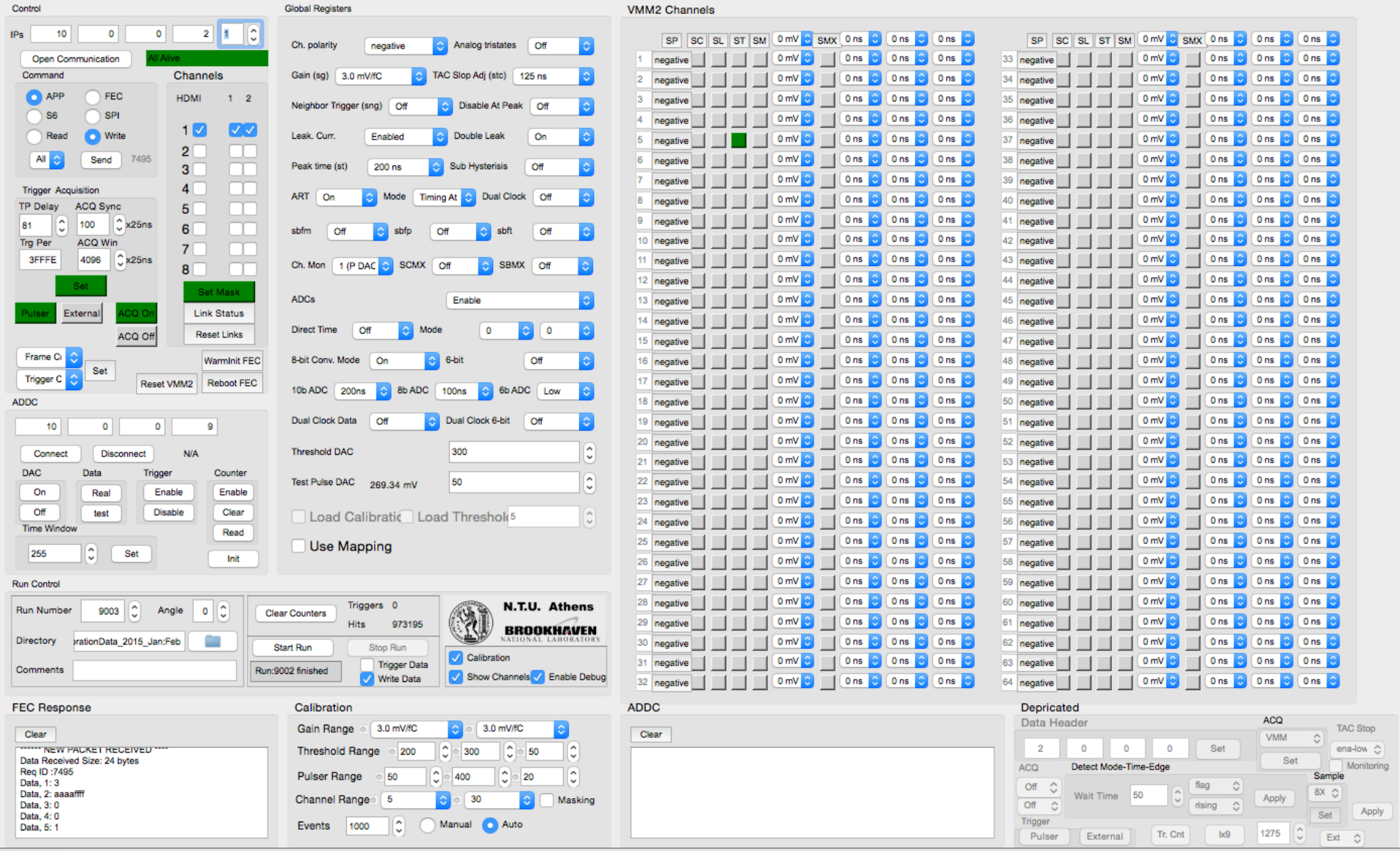
SRS

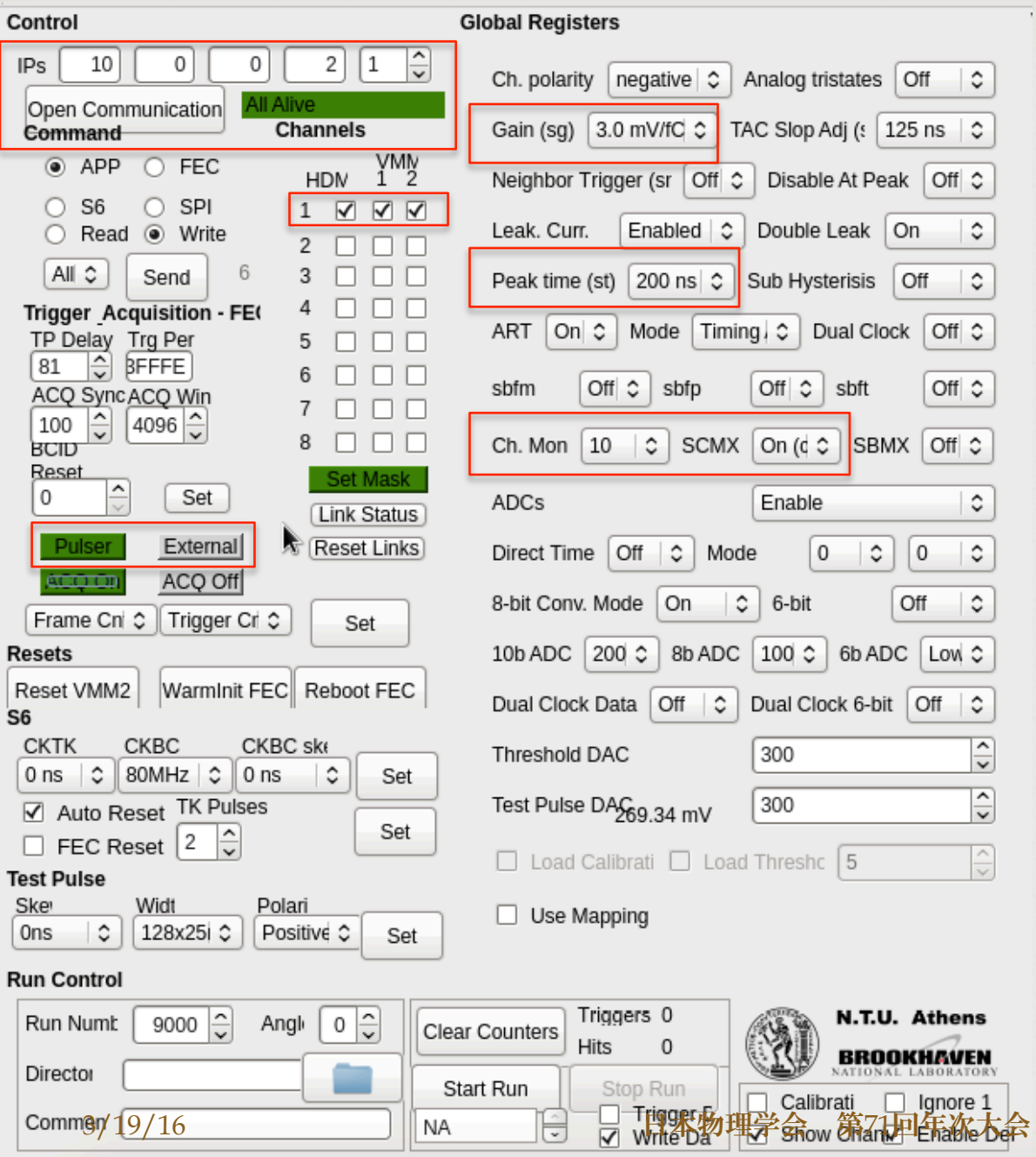
PC
NTU Athens

Ethernet



Analysis software
NTU Athens software – connect and control VMM2





Gain

It can select lots of gain as

0.5, 1, 3, 4.5. 6, 9, 12, 16 mV/fC

It could take Wider energy dynamic range

Peak time

It can select rise time Of signal
25, 50, 100, 200 ns

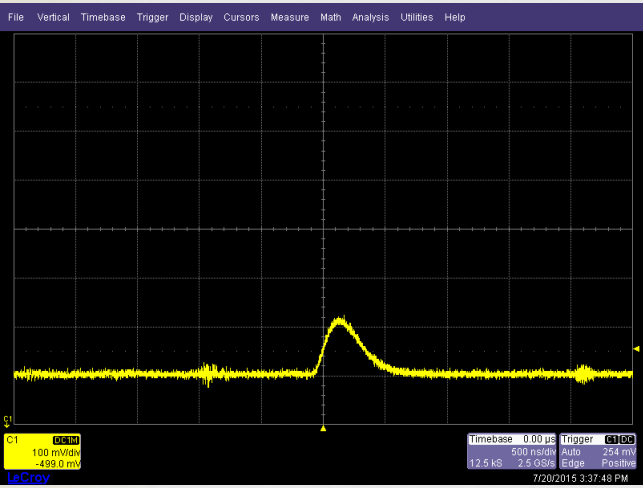
Monitoring channel

You can select channel
From 1 to 64 channel

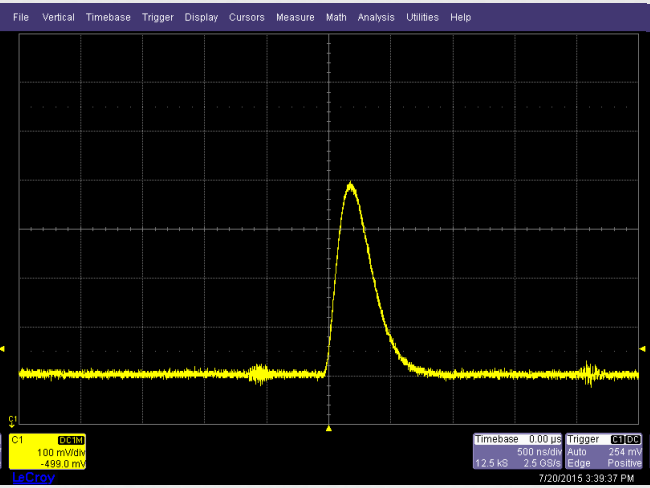
Results

Response check by internal Test Pulse DAC with oscilloscope

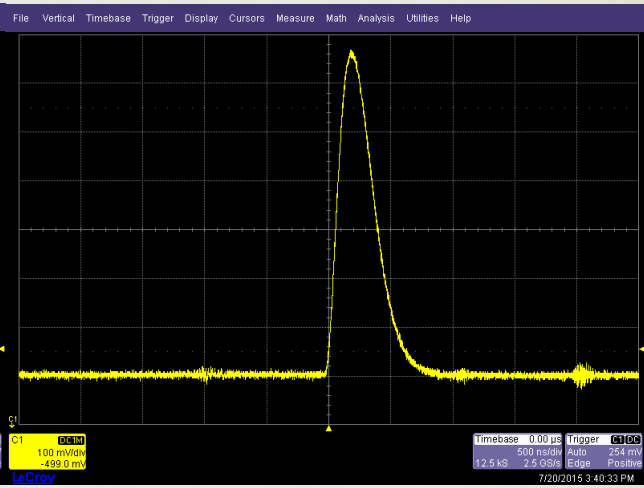
100 DAC

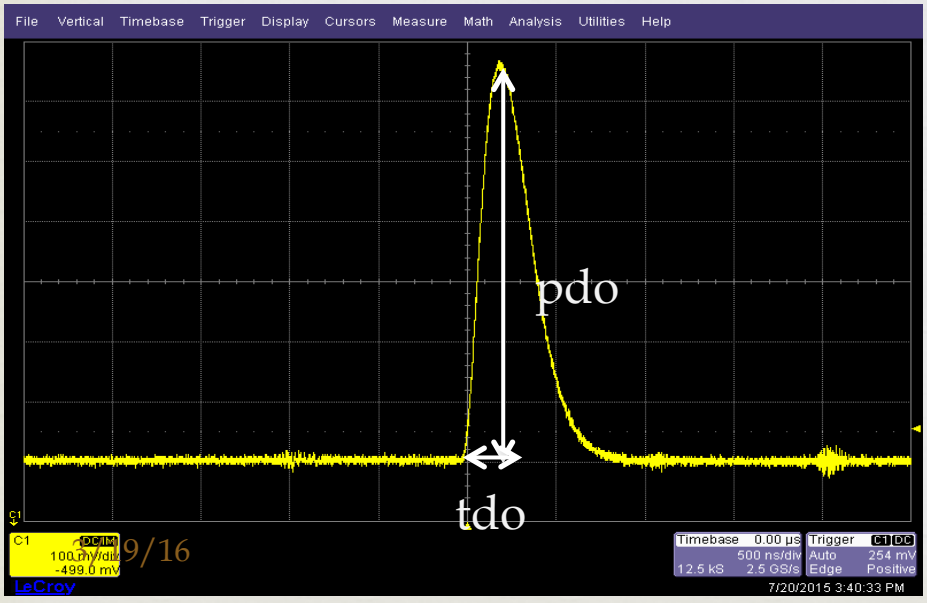


200 DAC



300 DAC





Pdo(peak detector output)

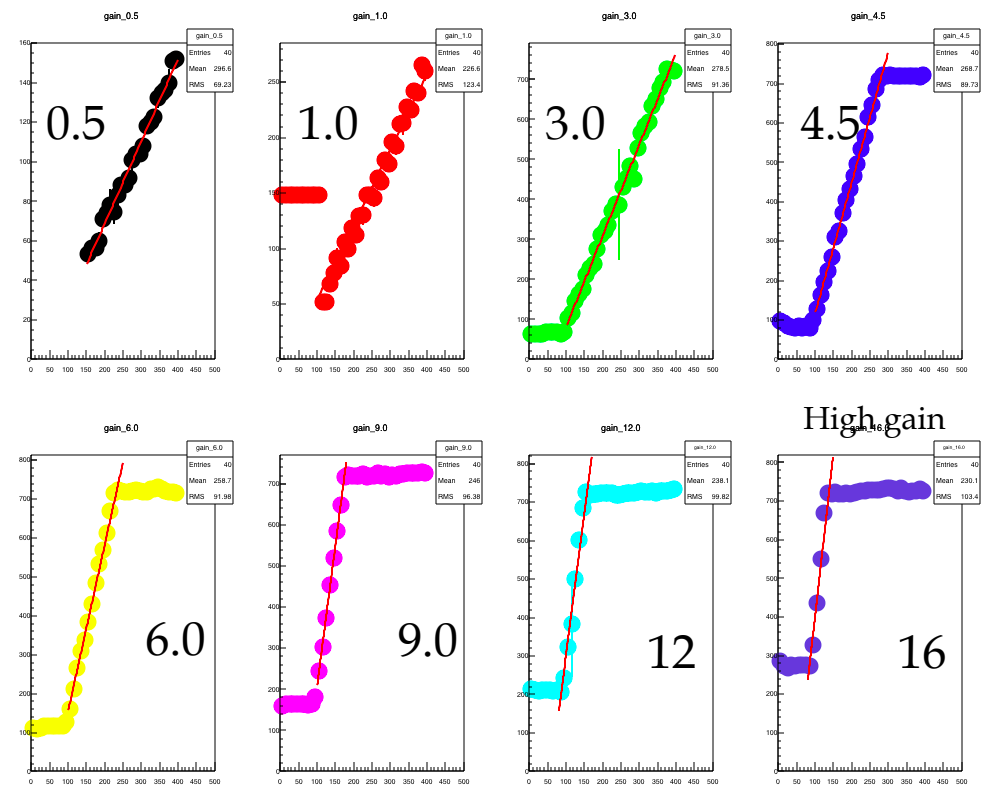
= return value of Amplitude

Tdo(time detector output)

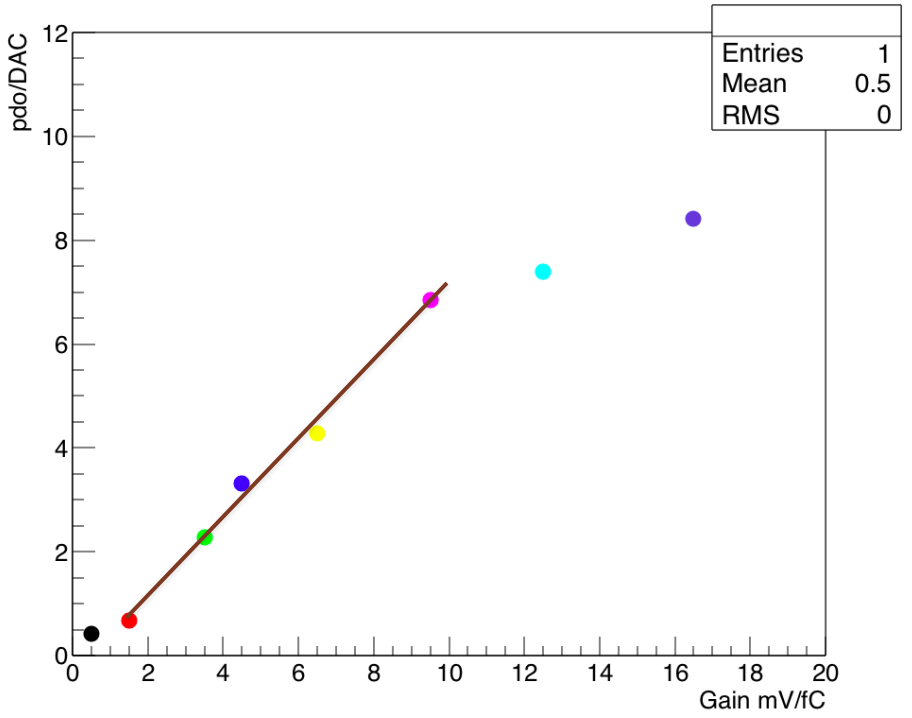
= return value of Rise time

Linearity check with internal test pulse by gain variation

Low gain

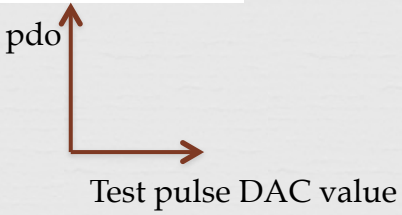


High gain



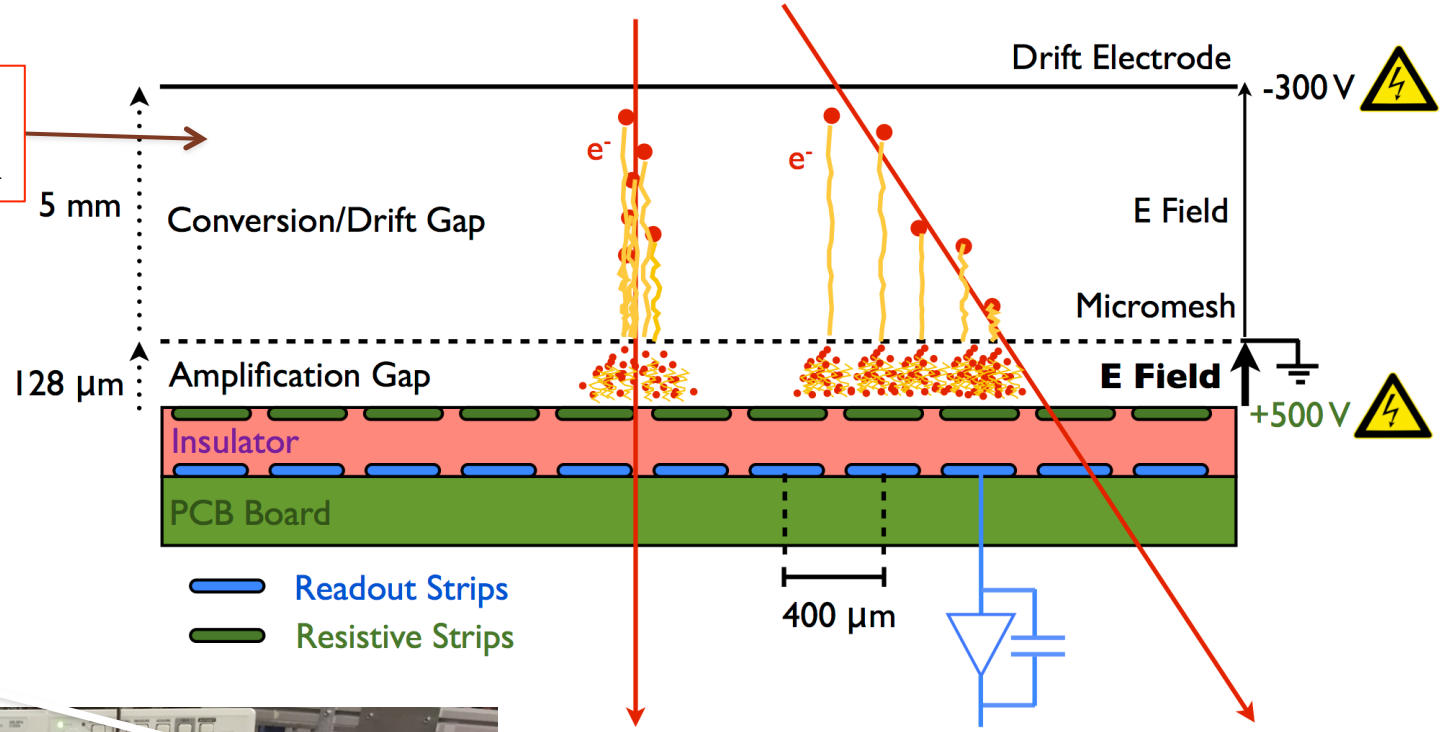
Gain 1.0 - 9.0 shows linearity.

Pdo vs Test pulse DAC value
Gain dependence
(0.5, 1.0, 3.0, 4.5, 6.0, 9.0, 12 16)

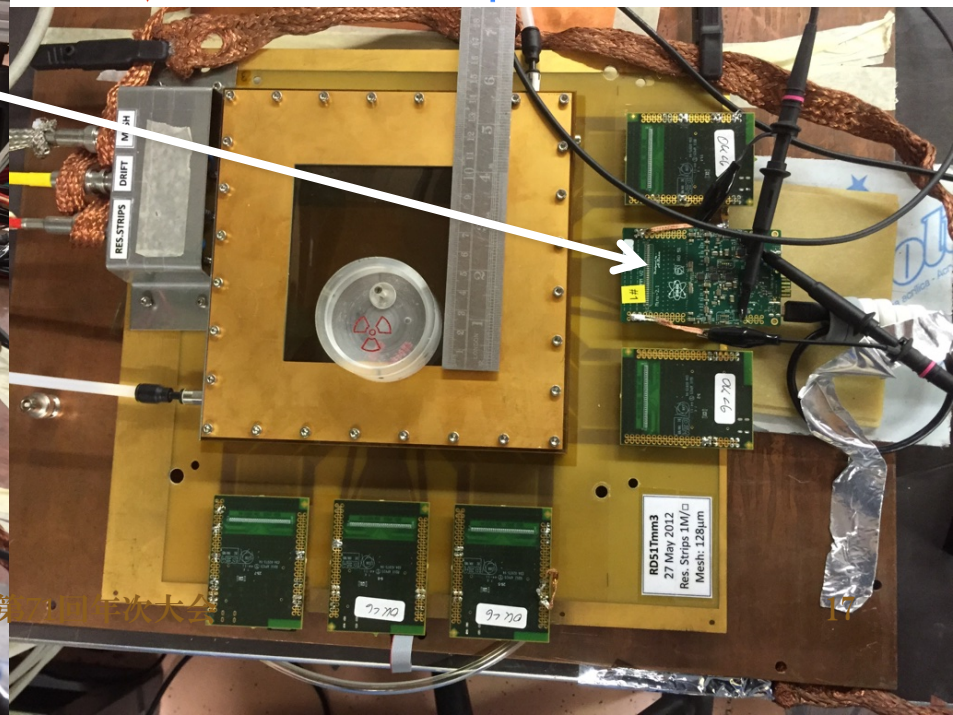


VMM test with Micro Megas

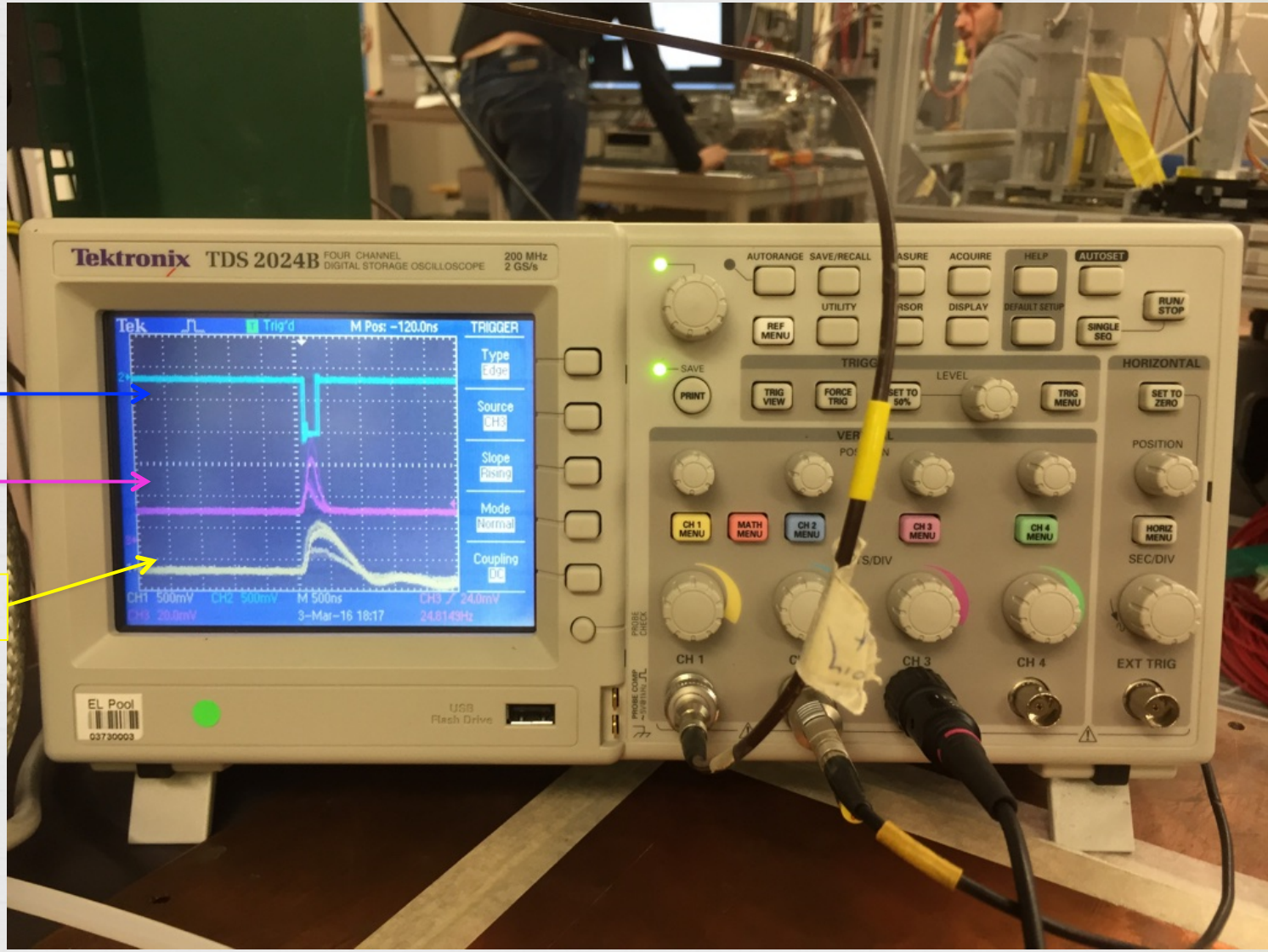
Gas electric field



VMM2 hybrid



VMM2 Response check With Micro Megas detector



Summary & out look

Summary

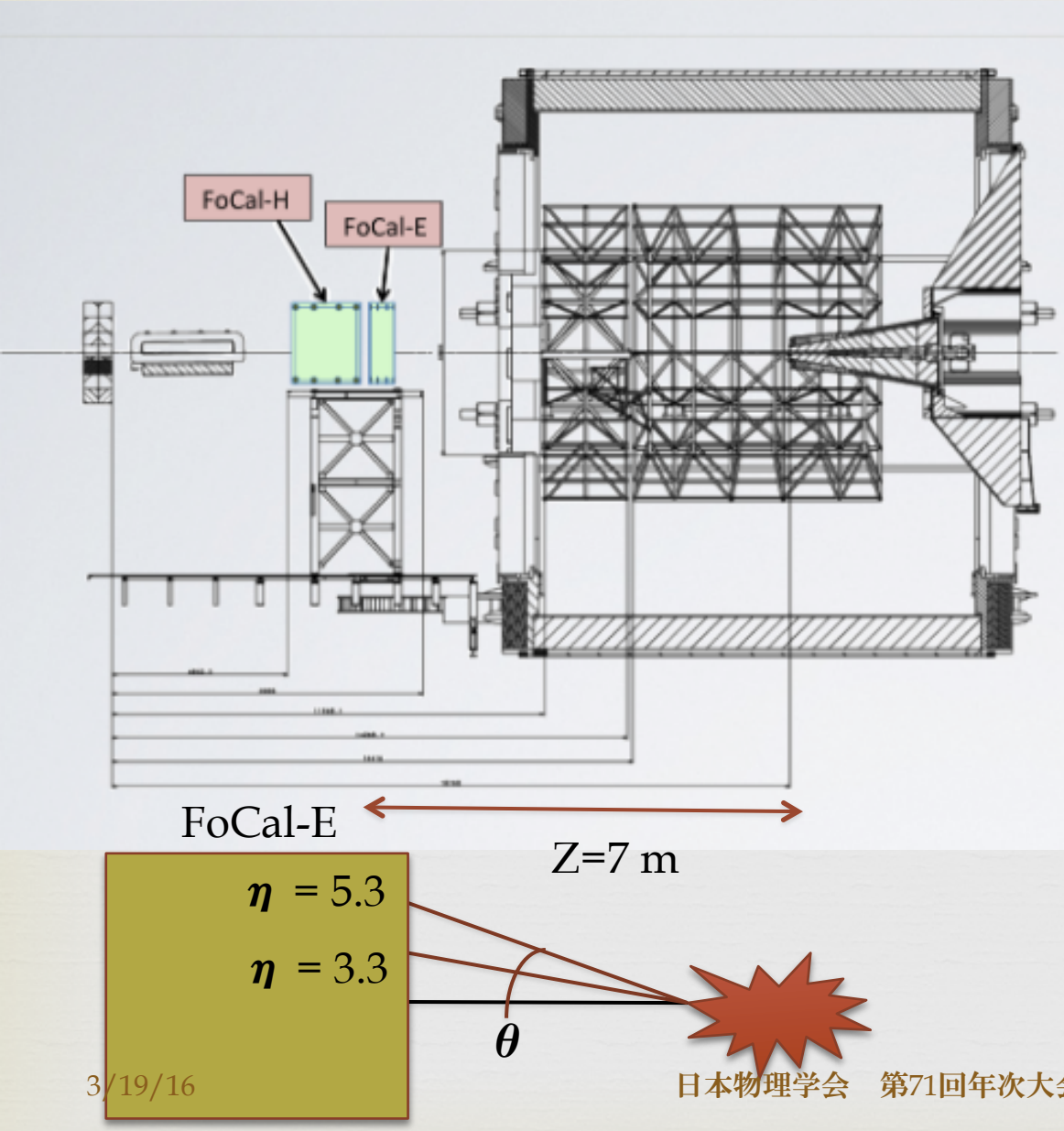
- Development & Research of new readout for FoCAl - E pad
- Built a test bench for VMM2 hybrid at RD51 lab
- Checked VMM2 hybrid response with internal , external pulse
- Tested VMM2 hybrid with Micro Megas detector

Out look

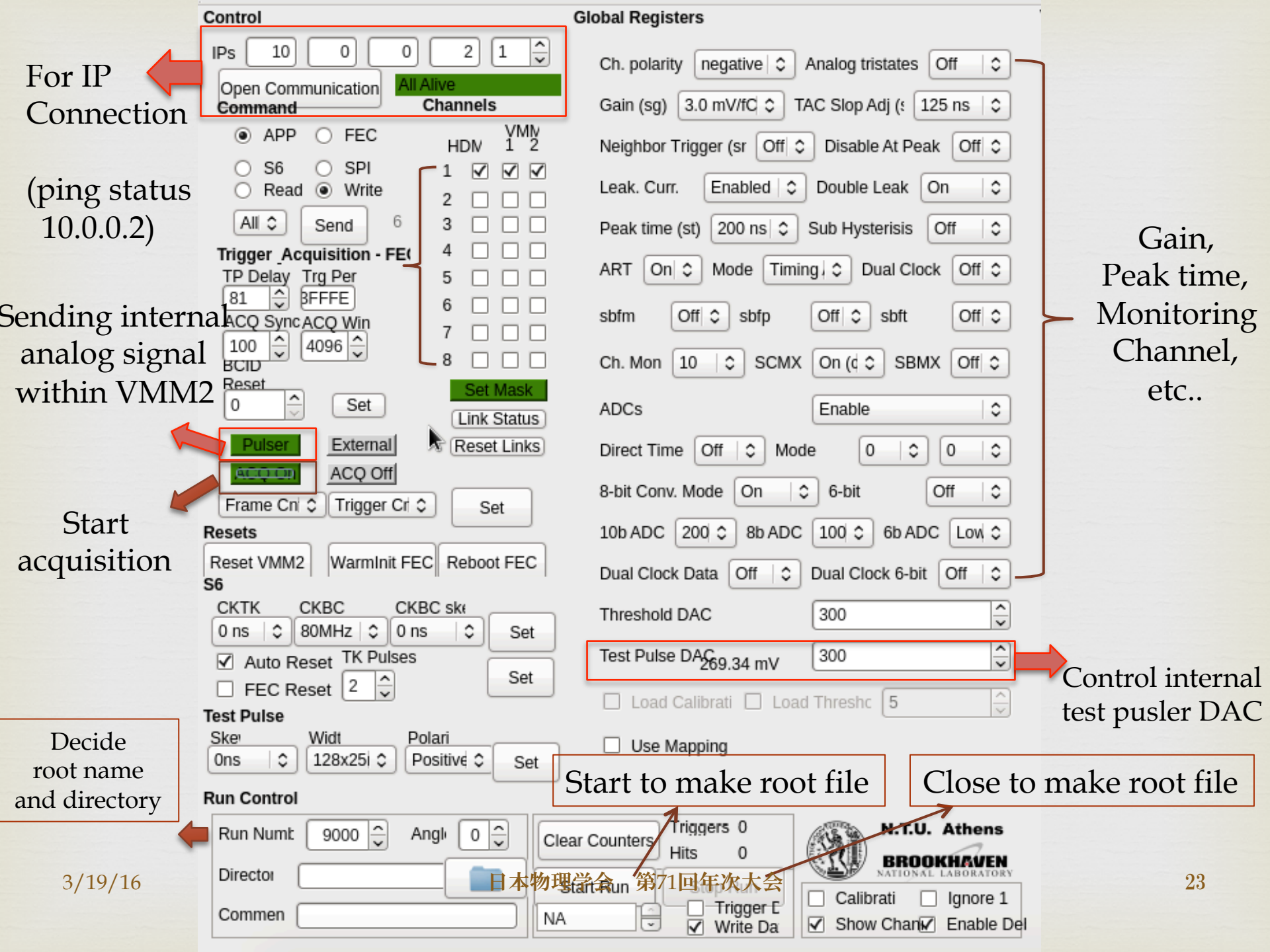
- development new software for test higher speed readout.
- VMM3(next version of VMM2) will be produced and tested as a new readout system.
- New LGL summing board toward VMM will be developed.
- Beam test will be conducted for FoCAl-E with VMM hybrid.

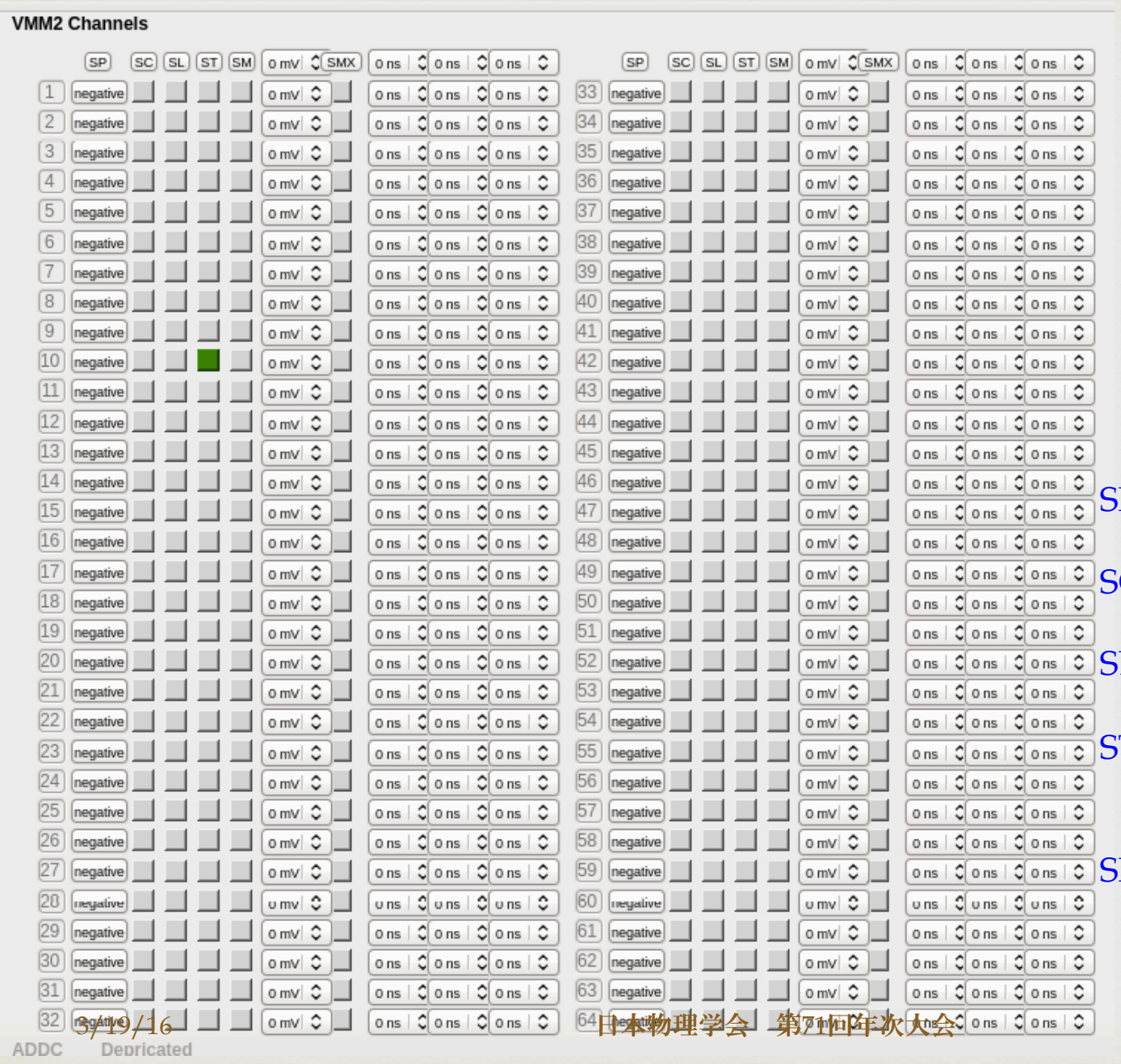
Back up

ALICE Upgrade Project – FoCal detector(toward LHC long shutdown at 2020years)



- location of installation
  - 7m at z direction from collision point.
- acceptance
  - $3.3 < \eta < 5.3$
- structure
  - electro-magnetic calorimeter (FoCal-E)
  - hadron calorimeter (FoCal-H)
- purpose
  - To Detect jet effect and direct photon at forward.


For IP Connection
(ping status 10.0.0.2)
Sending internal analog signal within VMM2
Start acquisition
Gain, Peak time, Monitoring Channel, etc..
Control internal test pusler DAC
Decide root name and directory
Start to make root file
Close to make root file
Control
Global Registers
IPs
Open Communication
All Alive
Command
Channels
APP
FEC
S6
SPI
Read
Write
Send
Trigger _Acquisition - FE(
TP Delay
Trg Per
ACQ Sync
ACQ Win
BCID Reset
Set
Set Mask
Link Status
Reset Links
Pulser
External
ACQ Off
Frame Cn
Trigger Cr
Resets
Reset VMM2
WarmInit FEC
Reboot FEC
S6
CKTK
CKBC
CKBC ske
Auto Reset
TK Pulses
FEC Reset
Test Pulse
Ske
Widt
Polari
Positive
Run Control
Run Numb
Angl
Director
Commen
Clear Counters
Triggers 0
Hits 0
Start Run
NA
Trigger E
Write Da
Ch. polarity
negative
Analog tristates
Off
Gain (sg)
3.0 mV/fC
TAC Slop Adj (s
125 ns
Neighbor Trigger (sr
Disable At Peak
Leak. Curr.
Enabled
Double Leak
On
Peak time (st)
200 ns
Sub Hysterisis
ART
Mode
Timing
Dual Clock
sbfm
sbfp
sbft
Ch. Mon
SCMX
SBMX
ADCs
Enable
Direct Time
Mode
8-bit Conv. Mode
6-bit
10b ADC
8b ADC
6b ADC
Dual Clock Data
Dual Clock 6-bit
Threshold DAC
Test Pulse DAC
269.34 mV
Load Calibrati
Load Threshc
Use Mapping
N.T.U. Athens
BROOKHAVEN NATIONAL LABORATORY
Calibrati
Ignore 1
Show Chan
Enable Del



64channels

Can be controlled

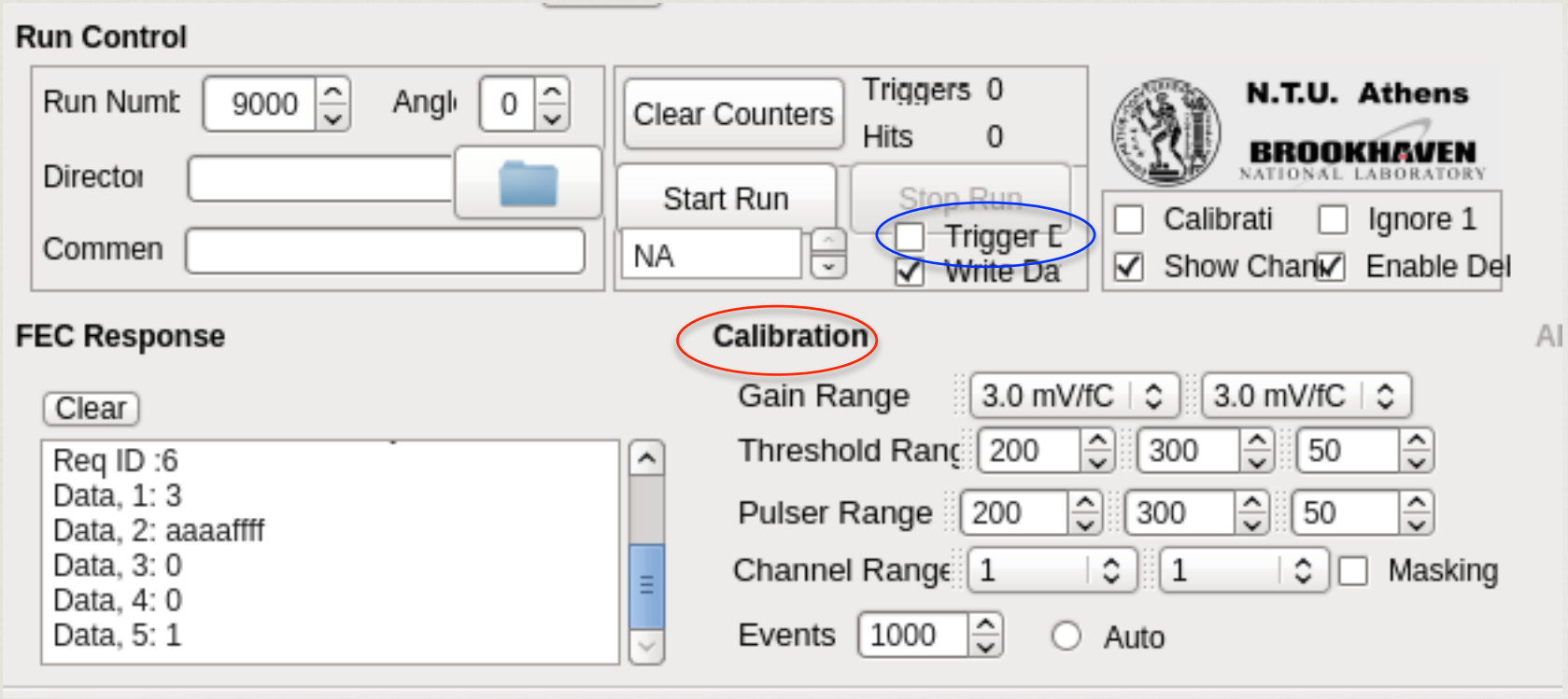
SP=adjustable polarity

SC=Sensor Capacitance

SL=Leakage Current disable

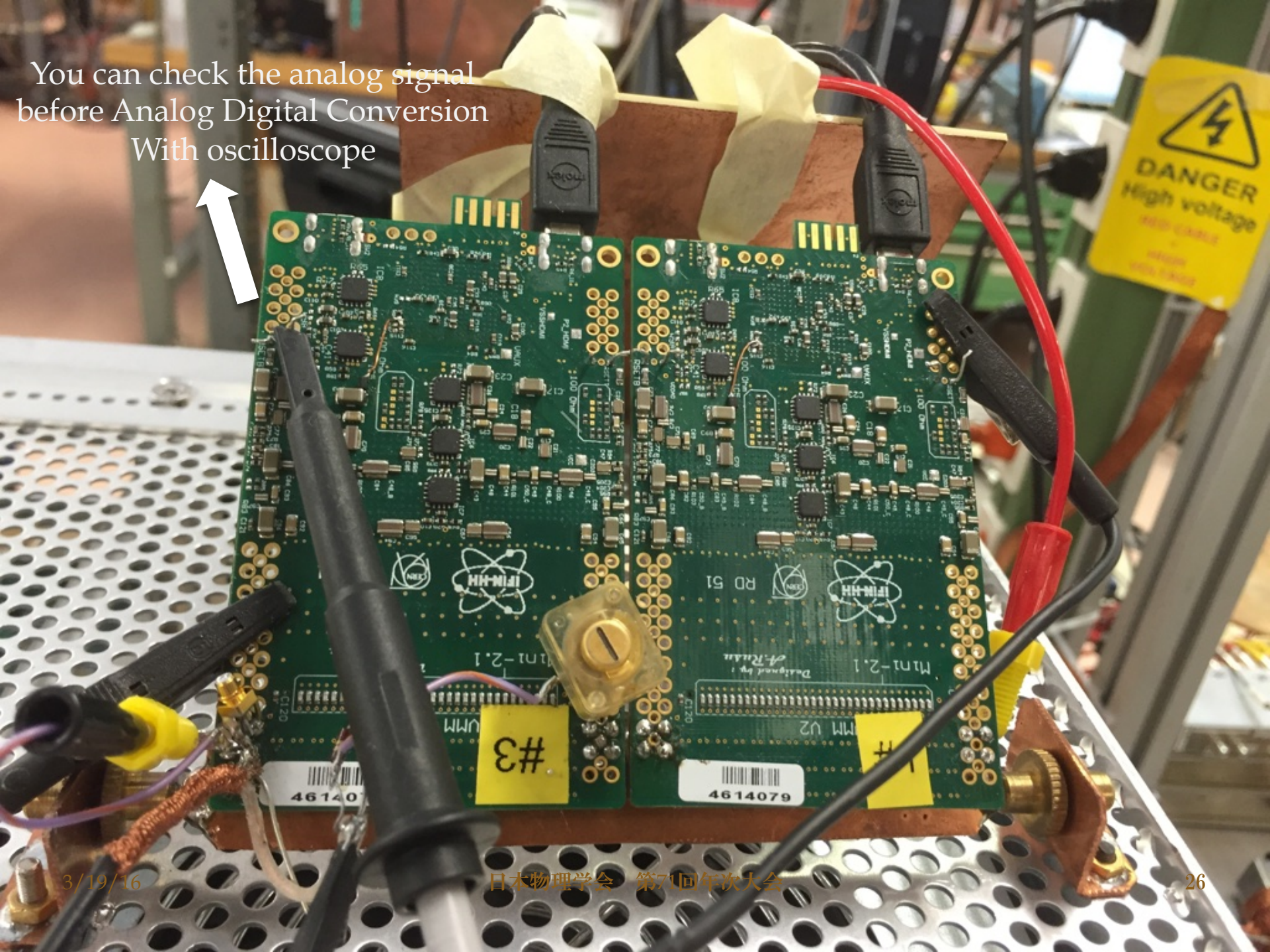
ST=1.2pF,Test Capacitor enable

SM=Mask enable

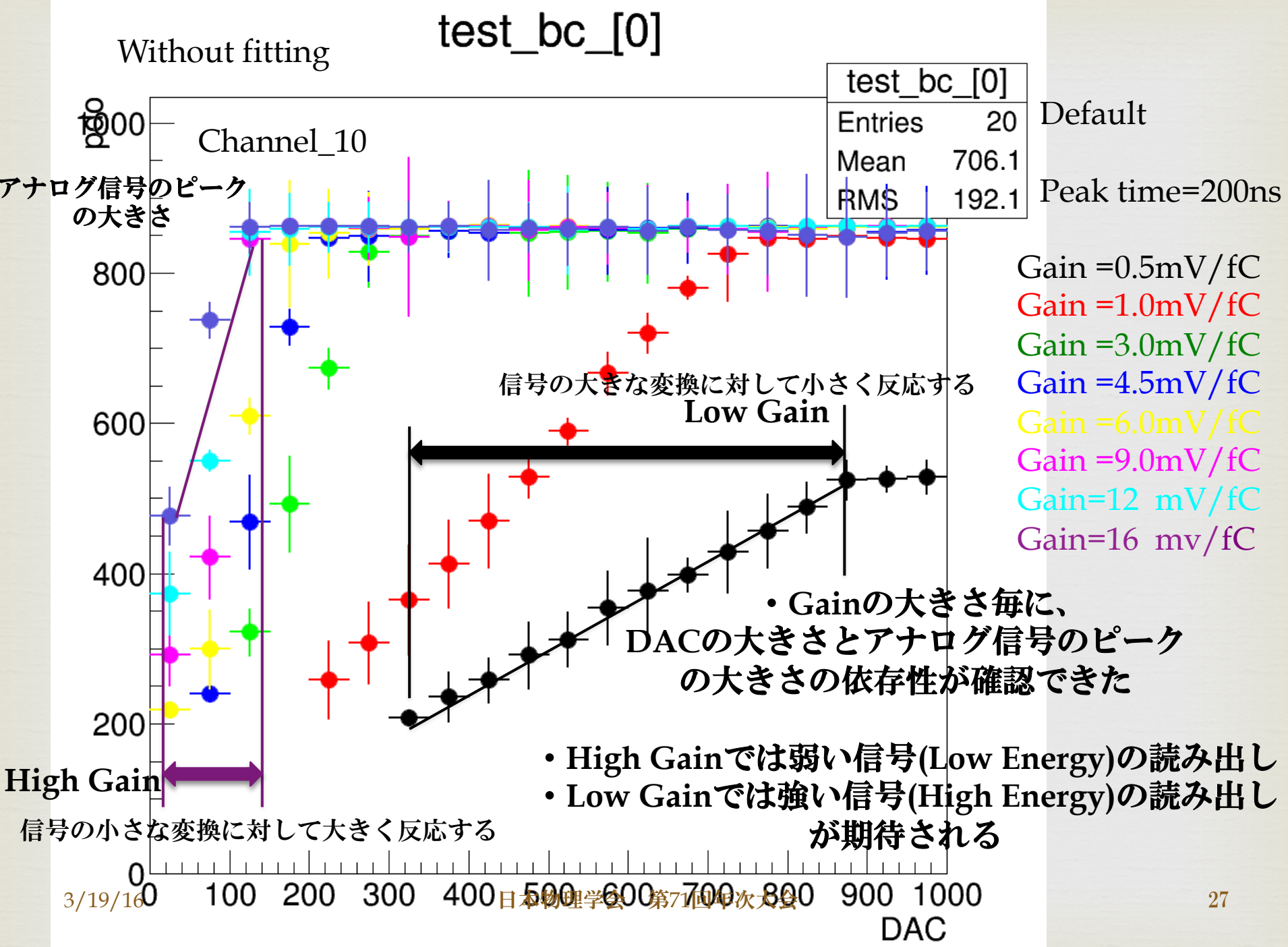


Calibration => It can make macros with internal test pulse.
Gain、Pulse range、channels 、Number of Events

Trigger Data => to observe response of VMM2 with external trigger


You can check the analog signal
before Analog Digital Conversion
With oscilloscope
DANGER
High voltage
#3
4614079

Without fitting



Default

Peak time=200ns

Gain =0.5mV/fC
Gain =1.0mV/fC
Gain =3.0mV/fC
Gain =4.5mV/fC
Gain =6.0mV/fC
Gain =9.0mV/fC
Gain=12 mV/fC
Gain=16 mv/fC

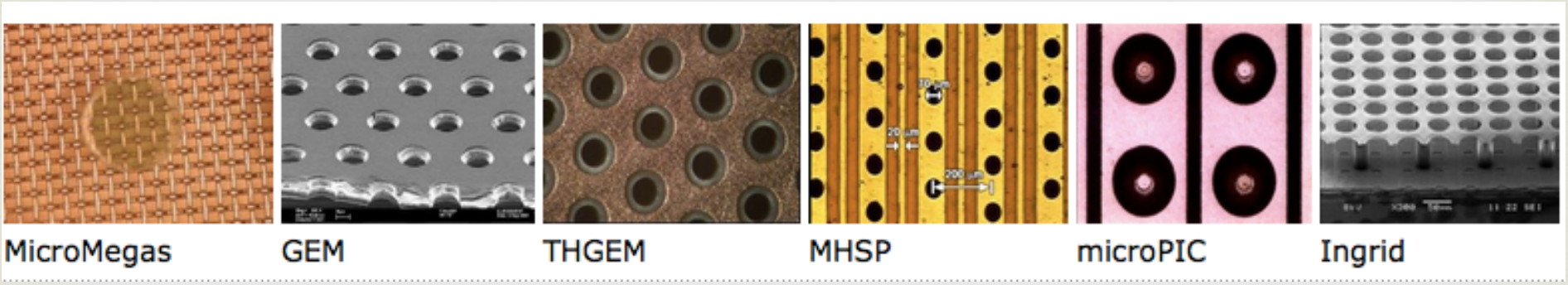
- Gainの大きさ毎に、DACの大きさとアナログ信号のピークの大きさの依存性が確認できた
- High Gainでは弱い信号(Low Energy)の読み出し
- Low Gainでは強い信号(High Energy)の読み出しが期待される

RD51 Collaborationの紹介
Development of Micro-Pattern Gas Detectors Technologies

- Micro Pattern Gas Detectors技術的発展とその応用を目指す。

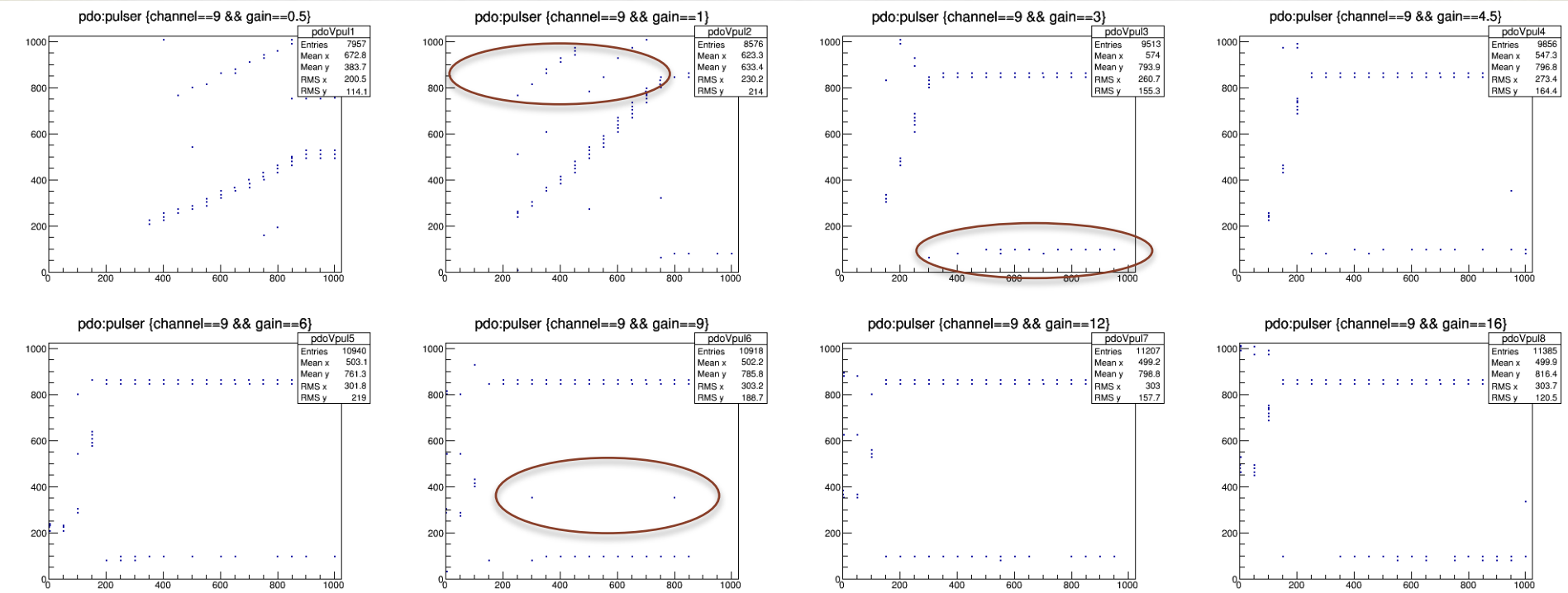
- その技術の基礎と応用された研究に向けて必要とされる electronic-readout systemの開発も行なっている。

- APV25 , VMM prototypeを開発した。



Some bugs of VMM

しかし、VMM2 prototype チップにはバグがある。

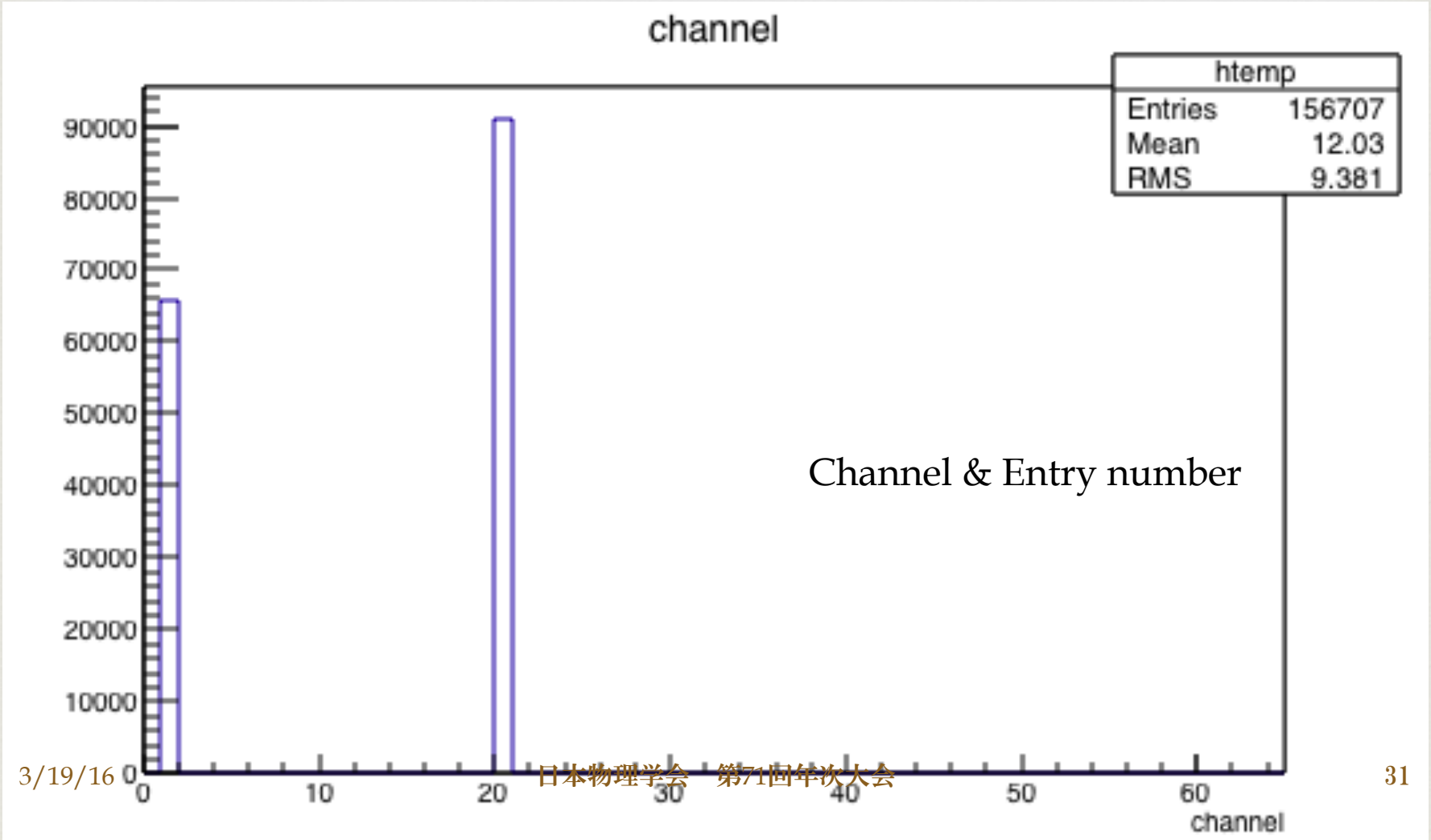


バグはどこからくるのか？

reason1) Cross talk　　reason2) bit flipping　　reason3) 原因が分からないバグ

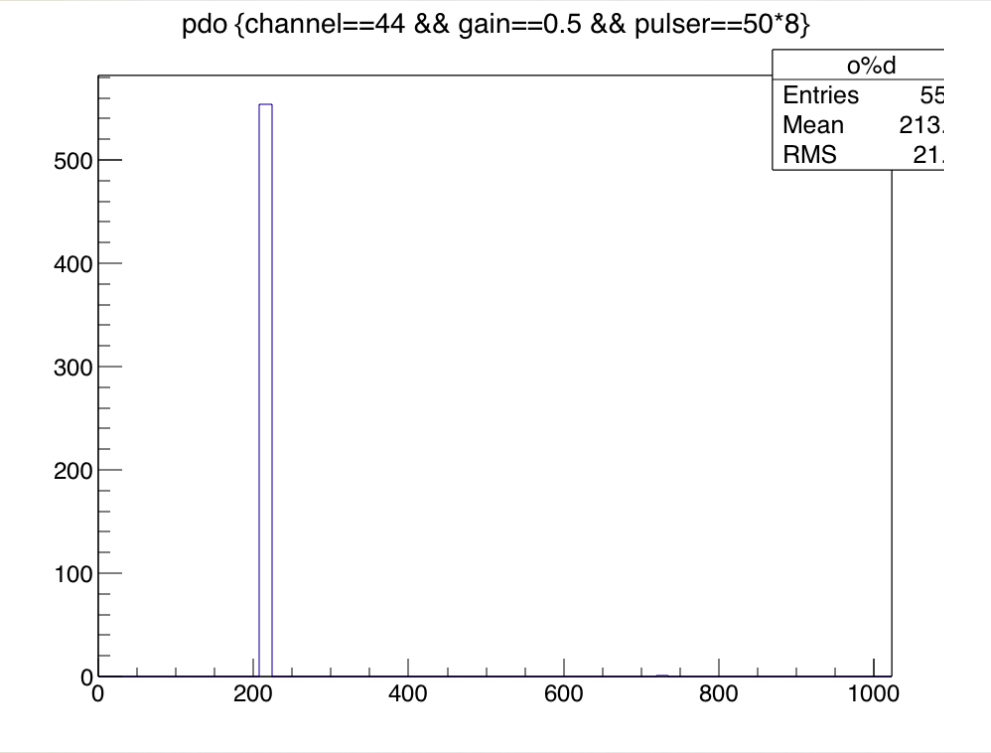
Reason 1) Cross talk (high gain and high Test Pulse DAC)

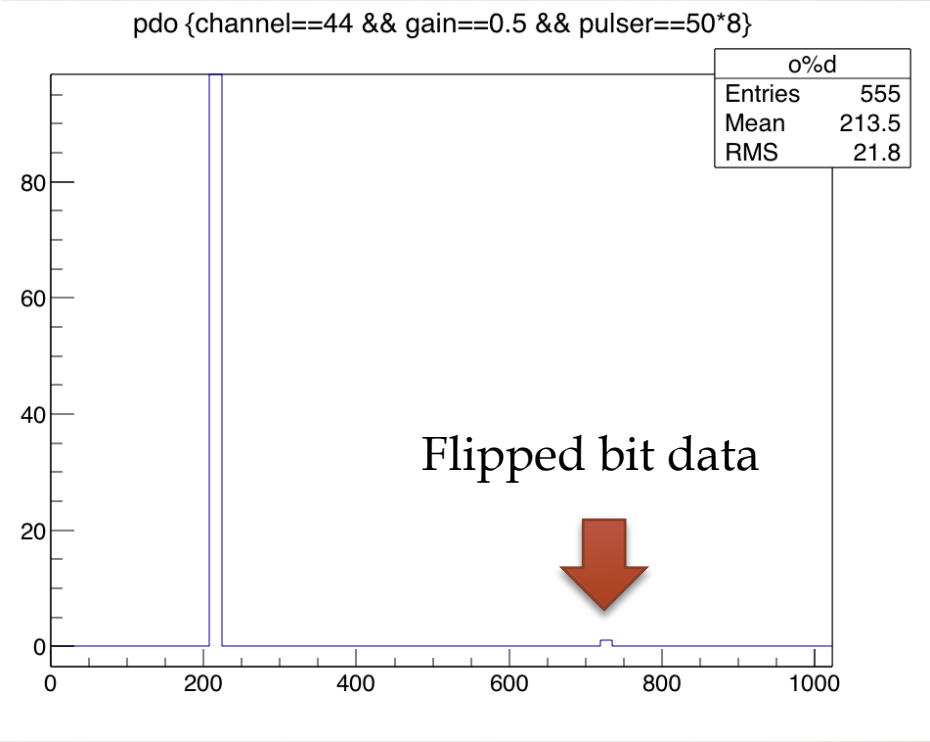
21チャンネルのみにアナログ信号を送った結果、違うチャンネルのでも反応をしていることが確認できた。



2) Bit flipping

Meanデータの倍数に信号が来るように見える現象があった。

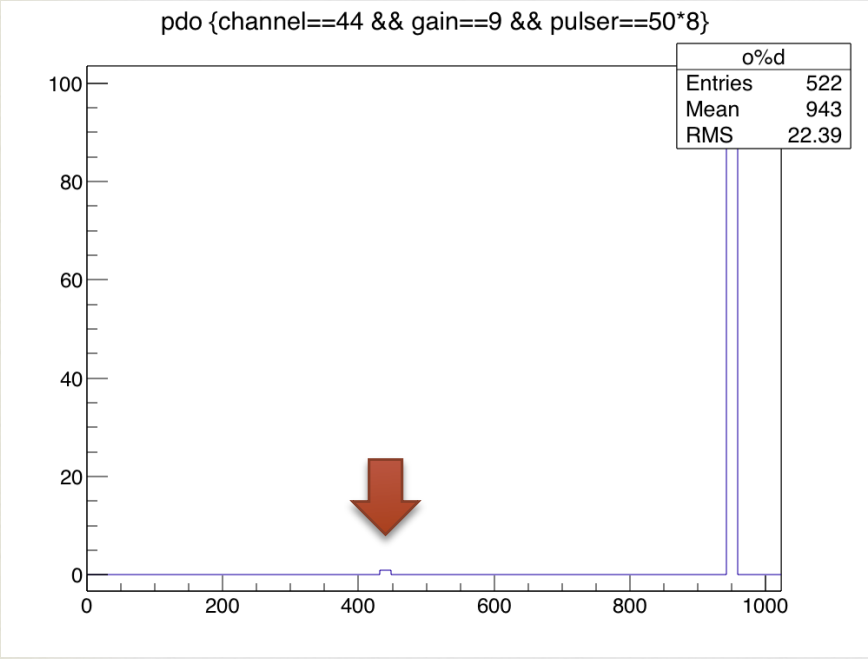


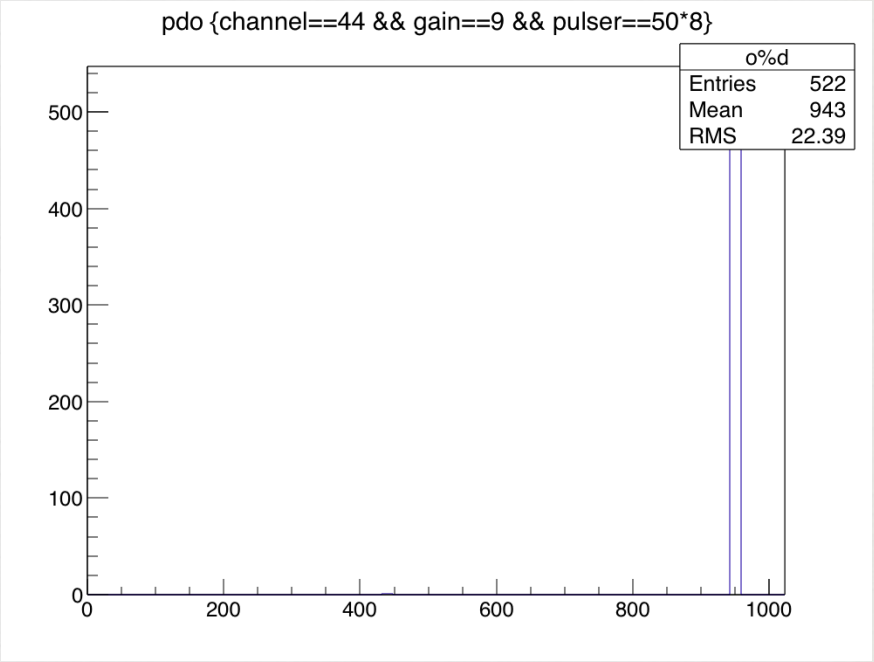


reason3) chip is bad.

Cross talkとBit flippingの現象以外にも原因が分からない

結果が見えた。この結果もprototypeのバグとして考えられる。

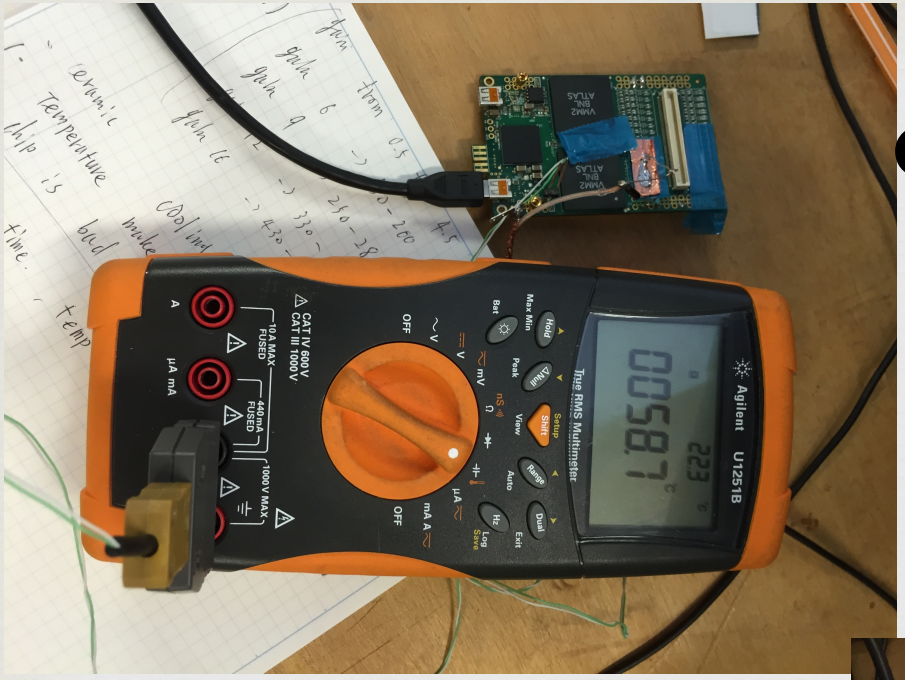


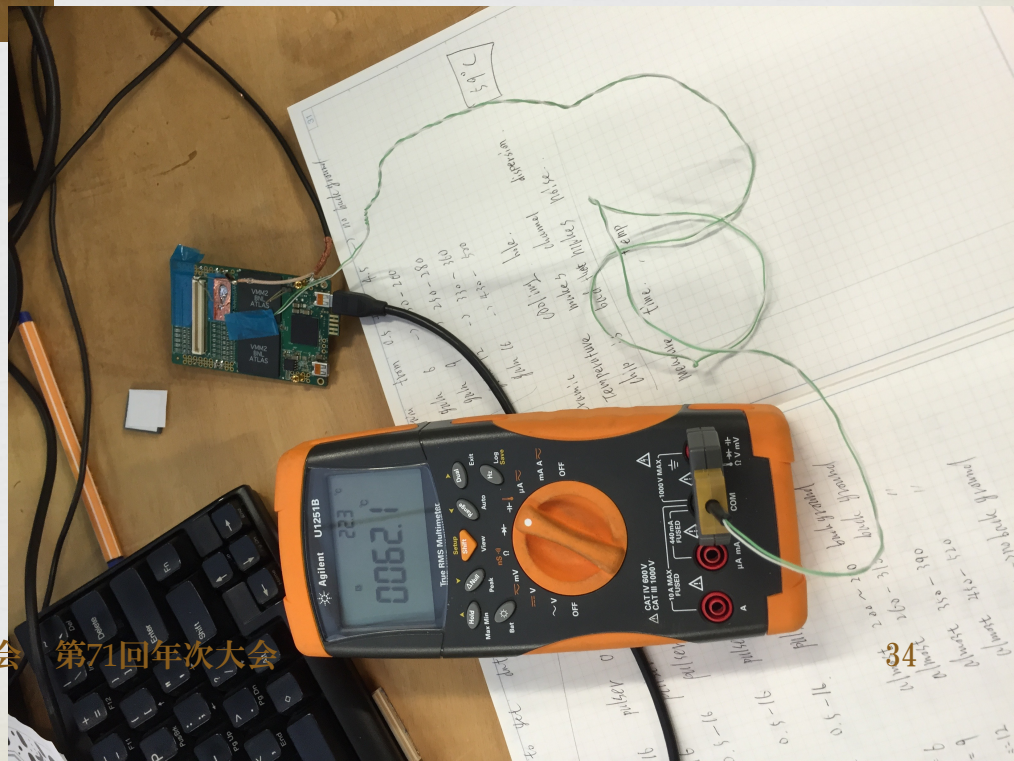


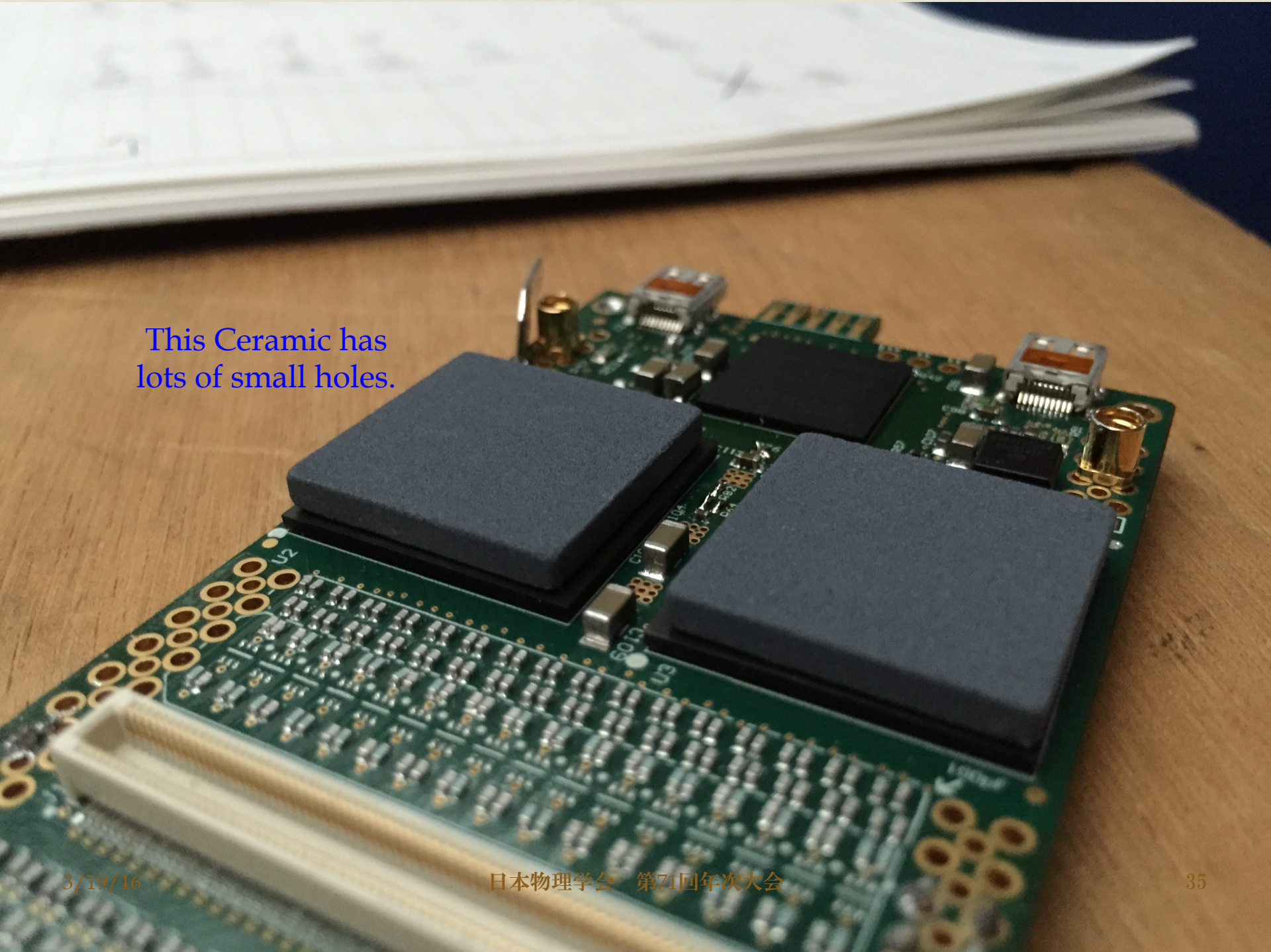
Check VMM2 Thermal data.

I tested thermal result of VMM2

With agilent u1251b.



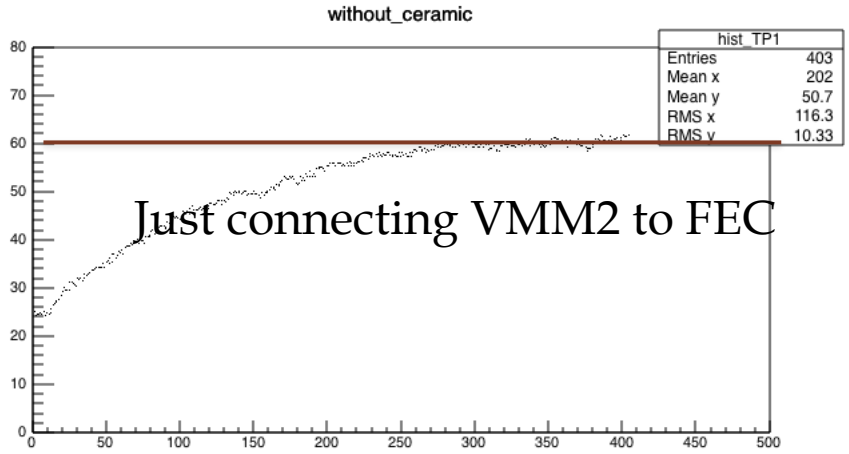


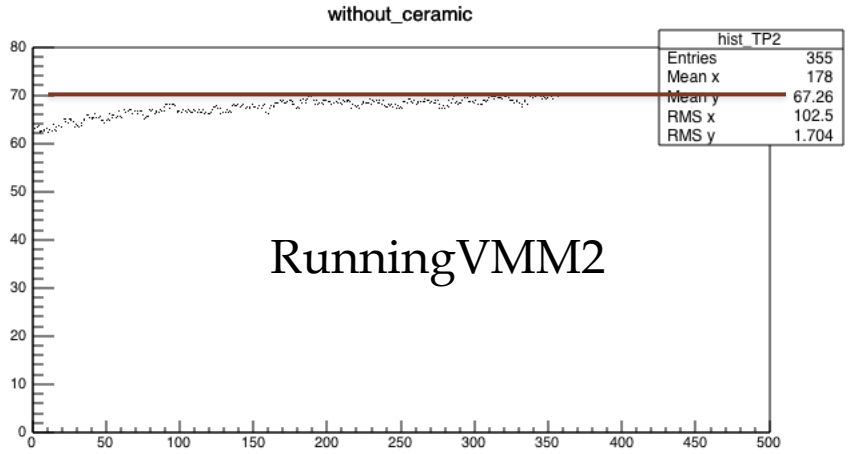

This Ceramic has
lots of small holes.

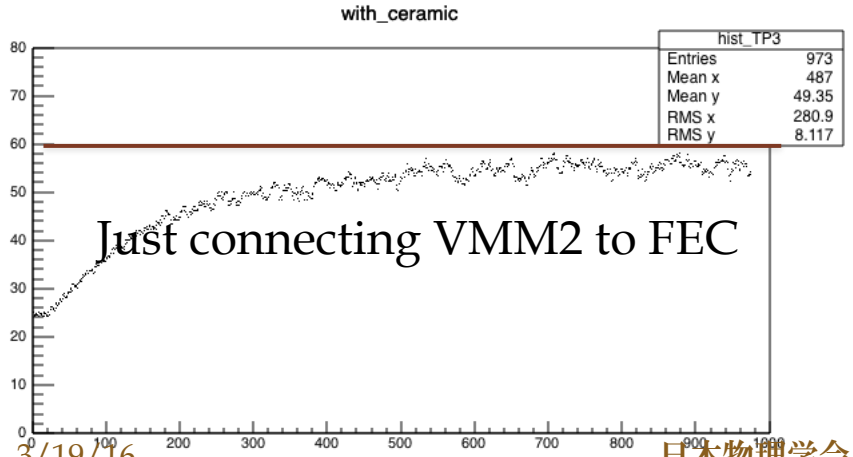
VMM2チップの温度が上がり、チップに損害を与える可能性があったため、温度低下のため、Ceramicを用いたVMM2チップの温度調節

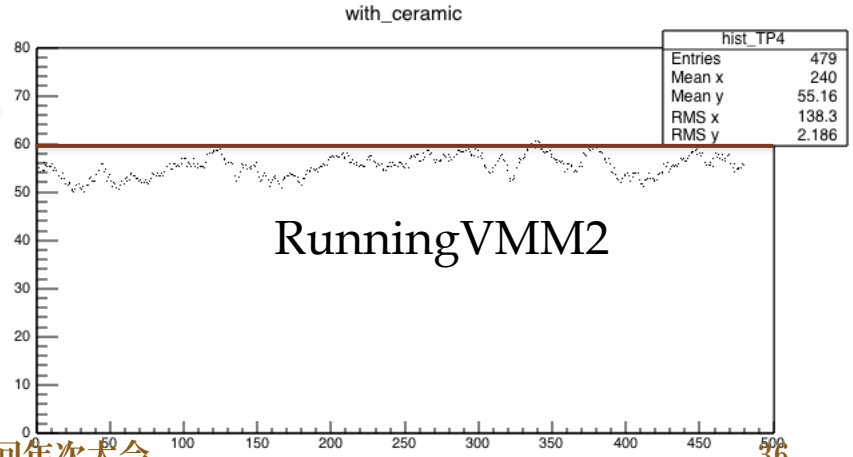
70℃->60℃

時間 Vs 温度





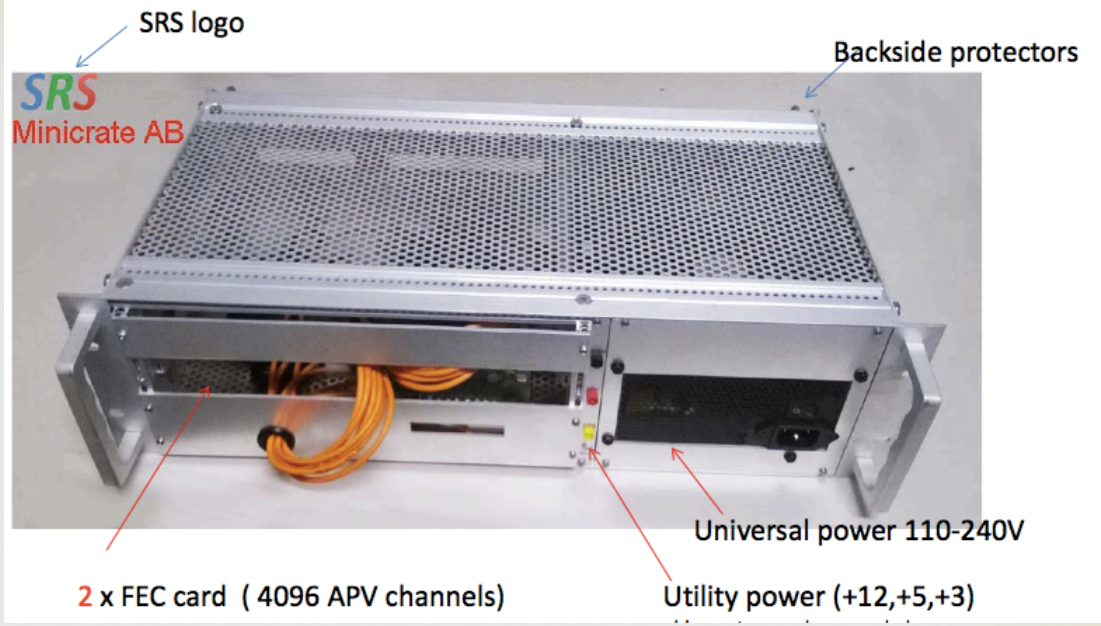




SRS System card

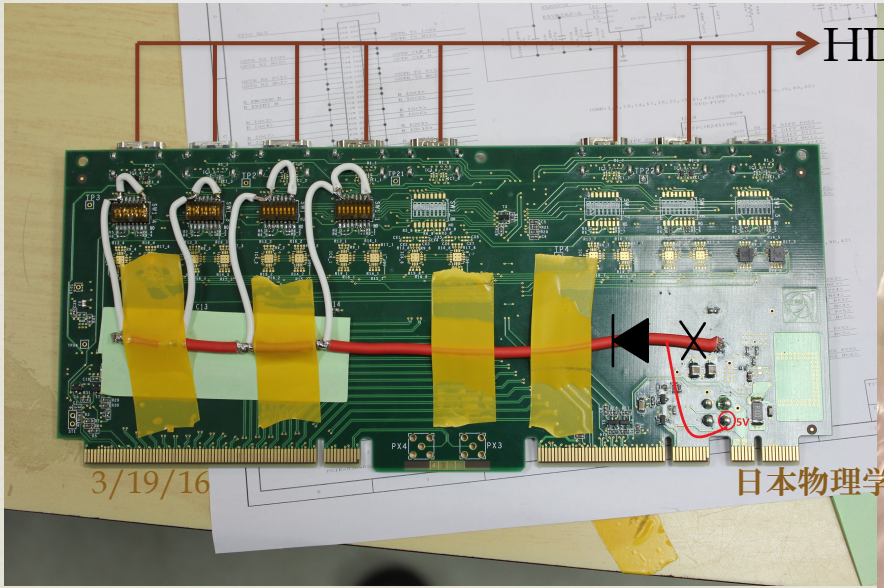
・D-CARD
<= VMM2から送られて来た
デジタル信号をFEC boardに送る。
<= VMM2に電力を提供する。
(VMM2の消費電力はAPV25の３倍)

・FEC V6
<= D-CARDからのデータを処理
し、PCへデータを送る。



電源モジュールを搭載した mini crate などをまとめたシステムのことである

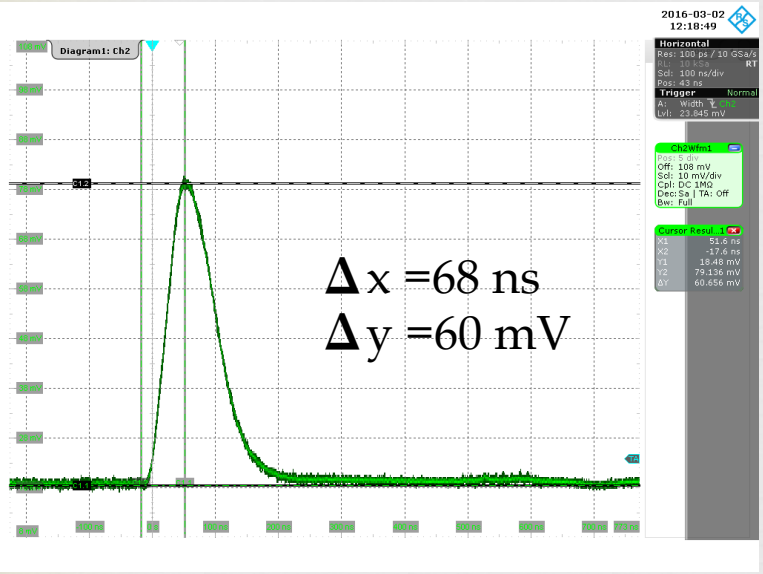
DCARD



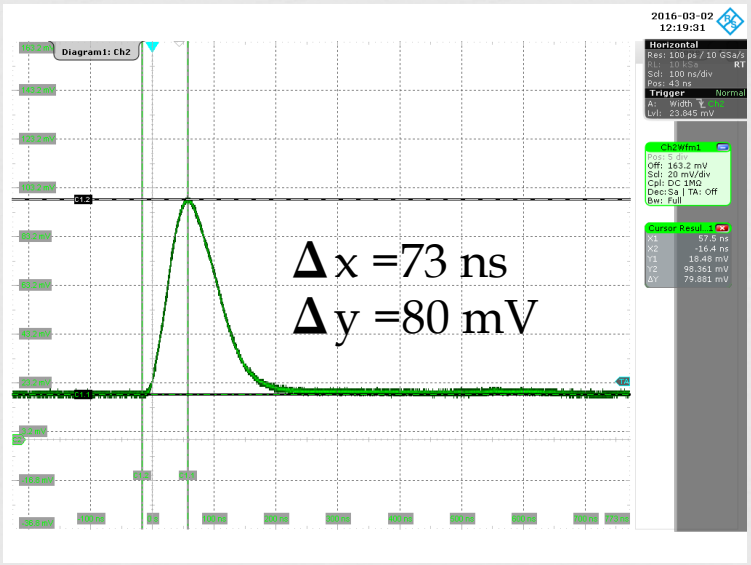
FEC V6

Analog response with internal pulser

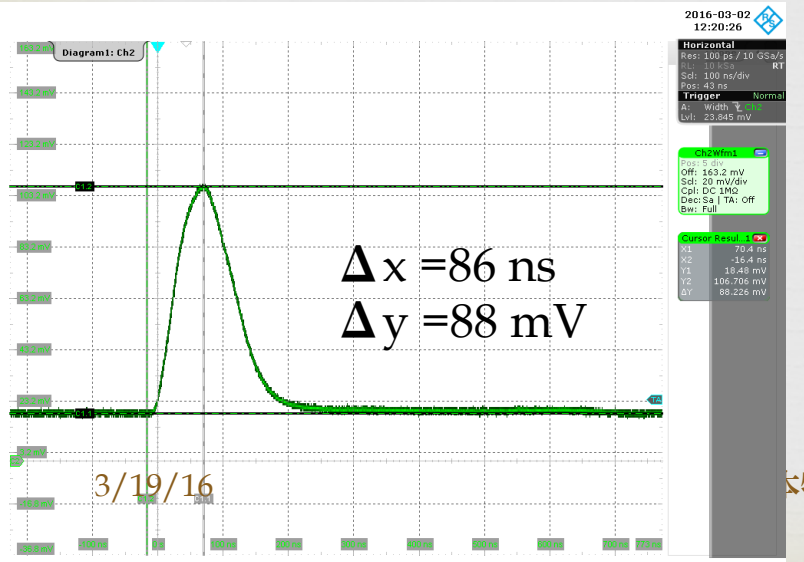
200



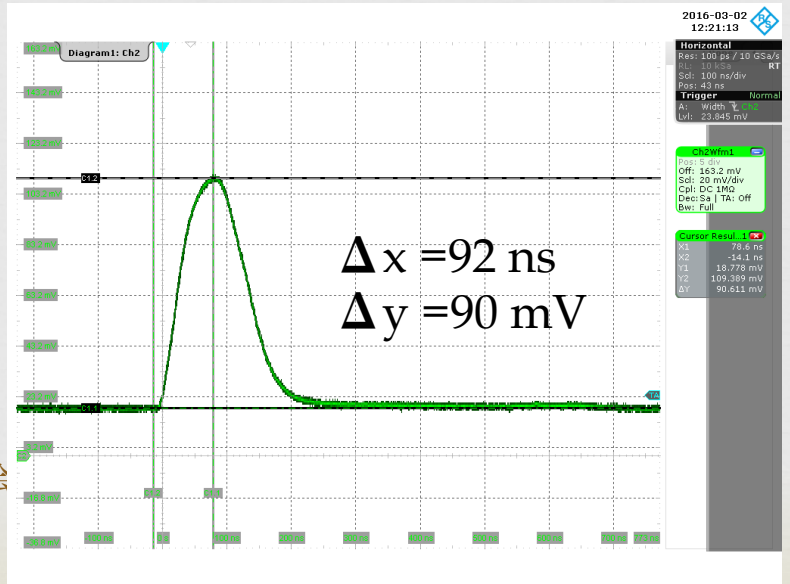
250



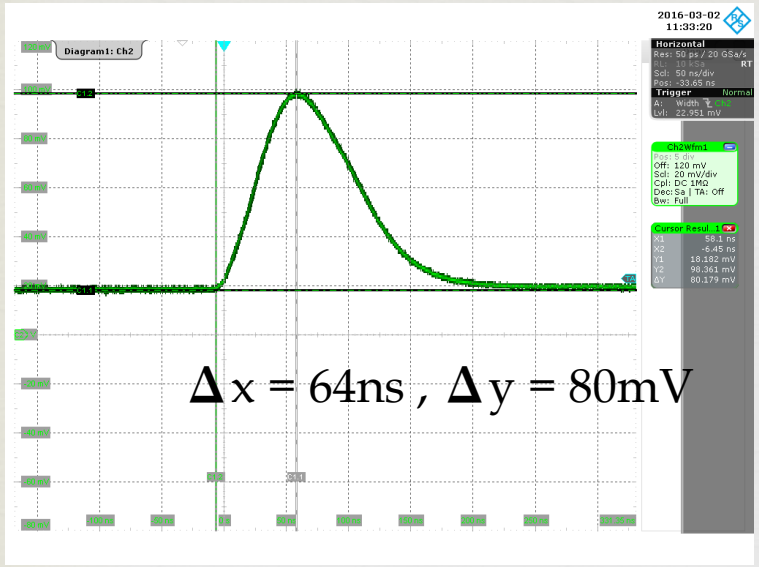
300



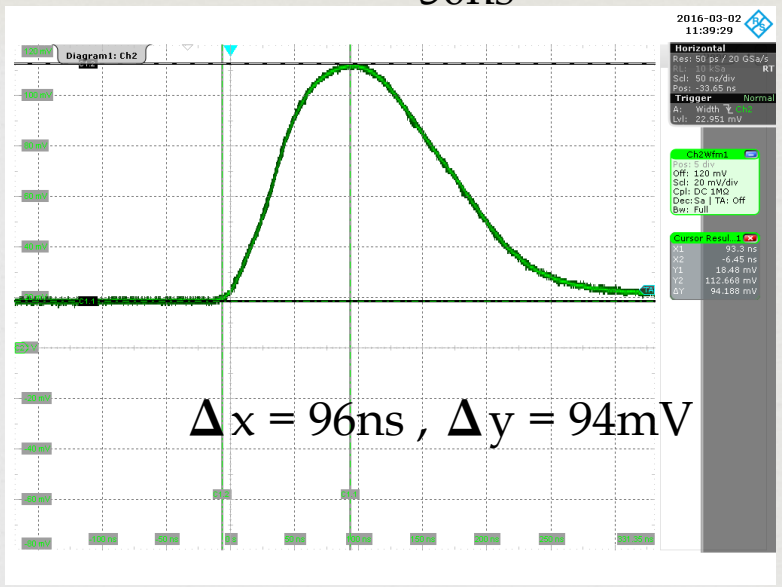
350



25ns

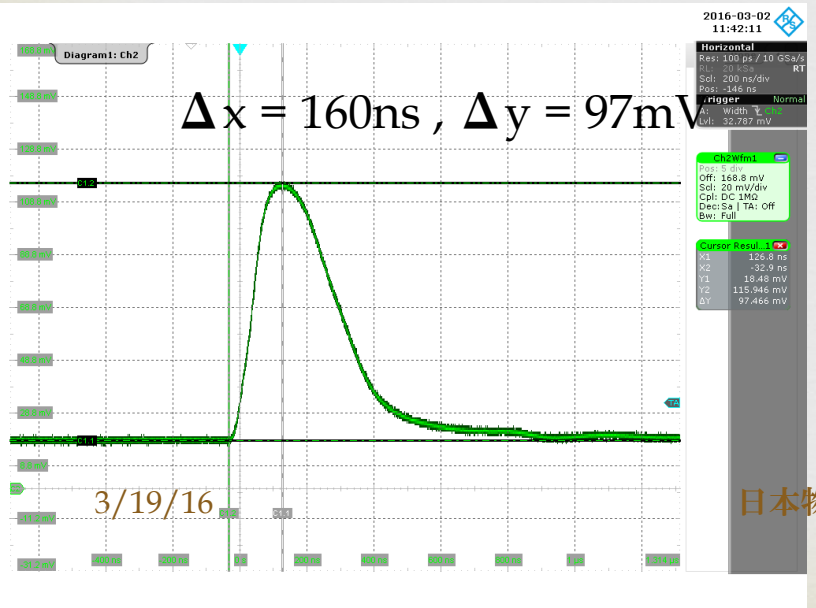


50ns

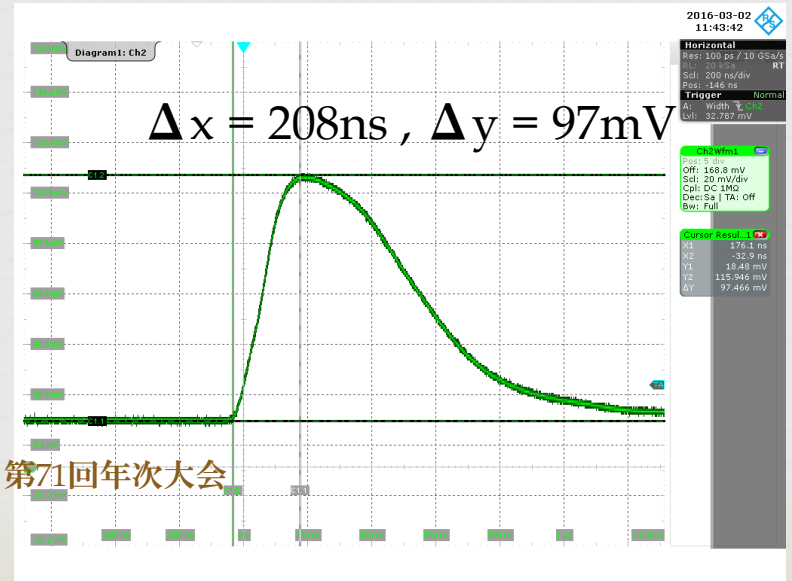


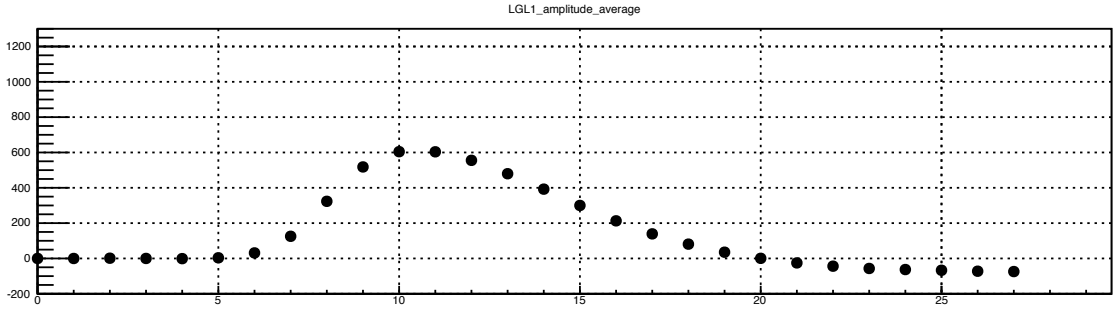
Gain 3.0 mV/fC , Test pulser DAC 400

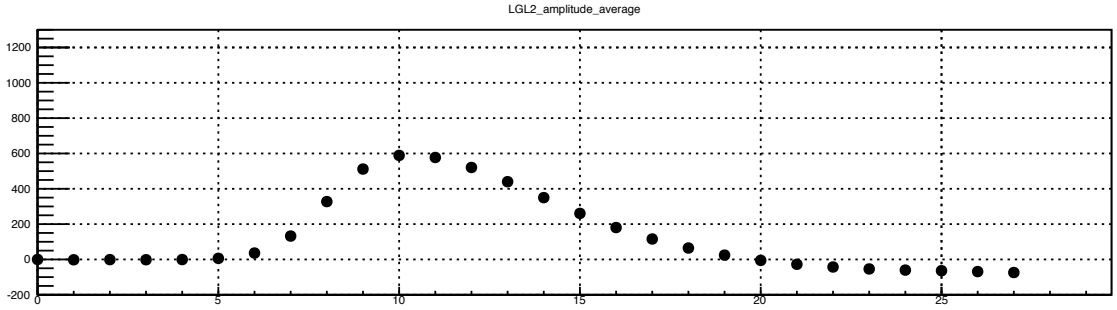
100ns

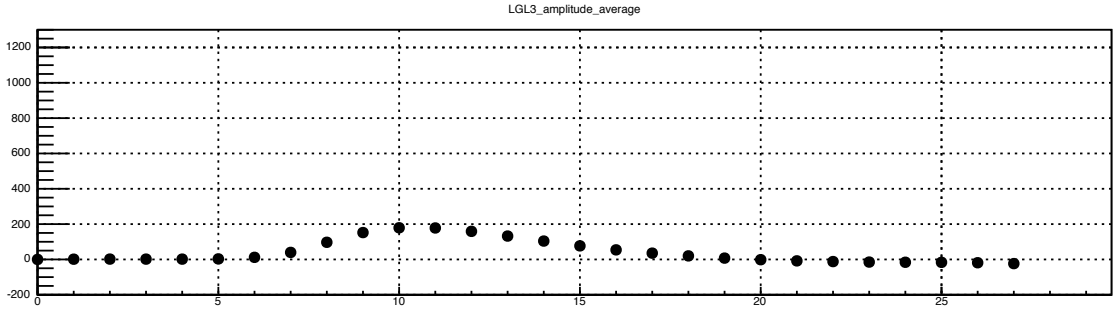


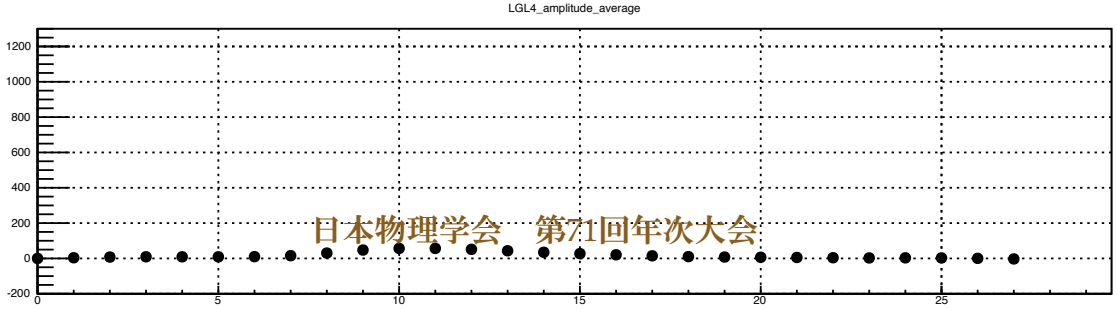
200ns




LGL1_amplitude_average
1200
1000
800
600
400
200
0
-200
0
5
10
15
20
25

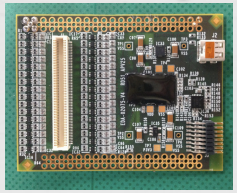

LGL2_amplitude_average
1200
1000
800
600
400
200
0
-200
0
5
10
15
20
25

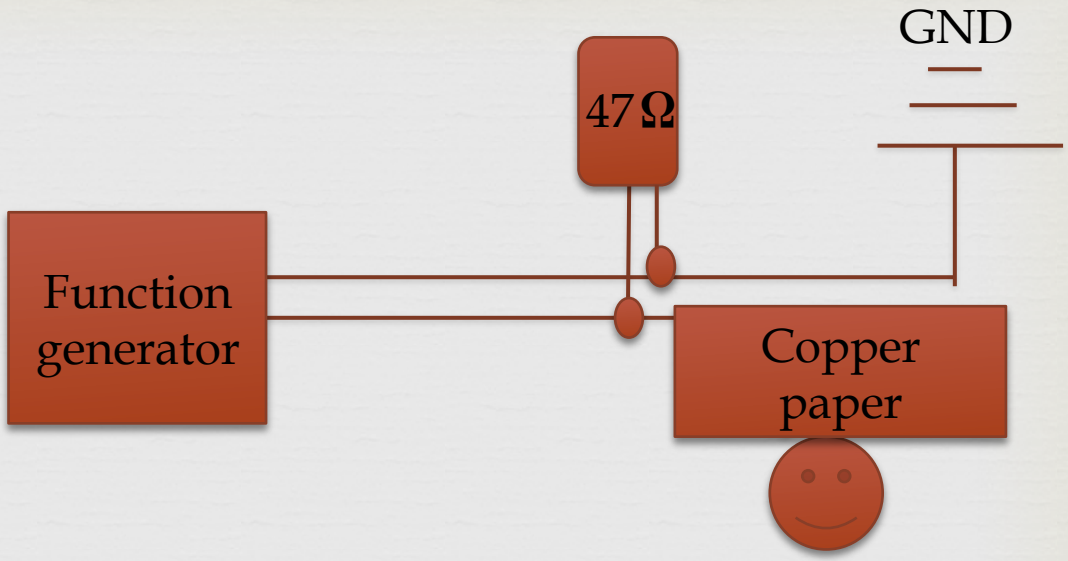

LGL3_amplitude_average
1200
1000
800
600
400
200
0
-200
0
5
10
15
20
25


LGL4_amplitude_average
1200
1000
800
600
400
200
0
-200
0
5
10
15
20
25

Nim Cable

VMM2 chip

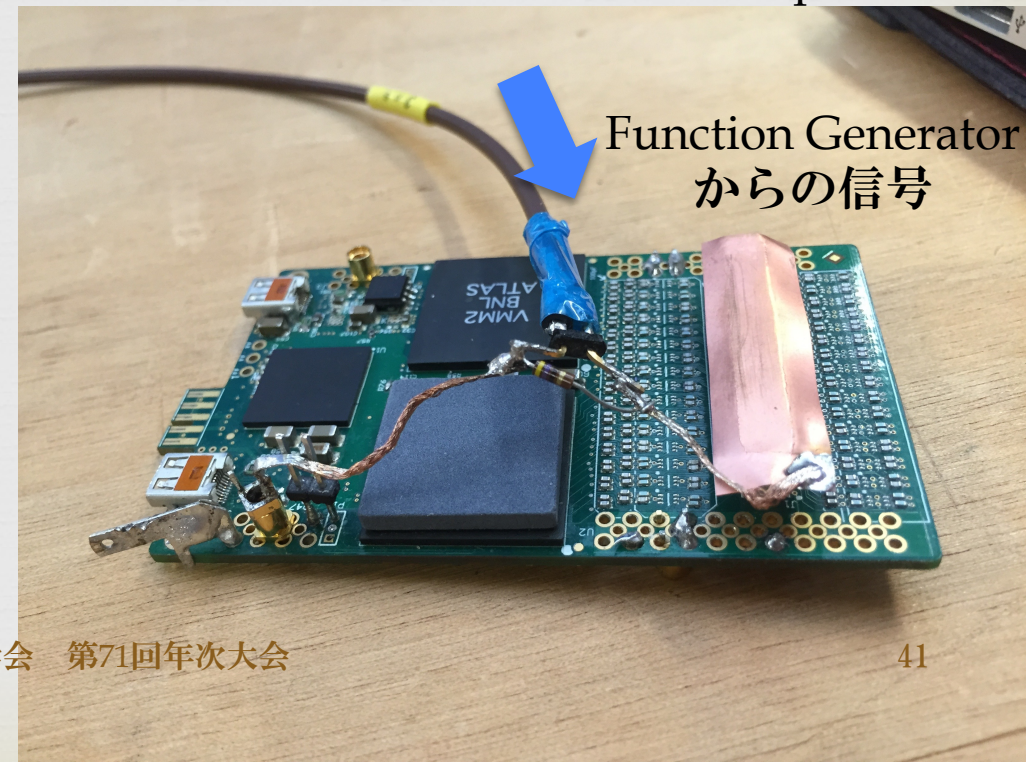


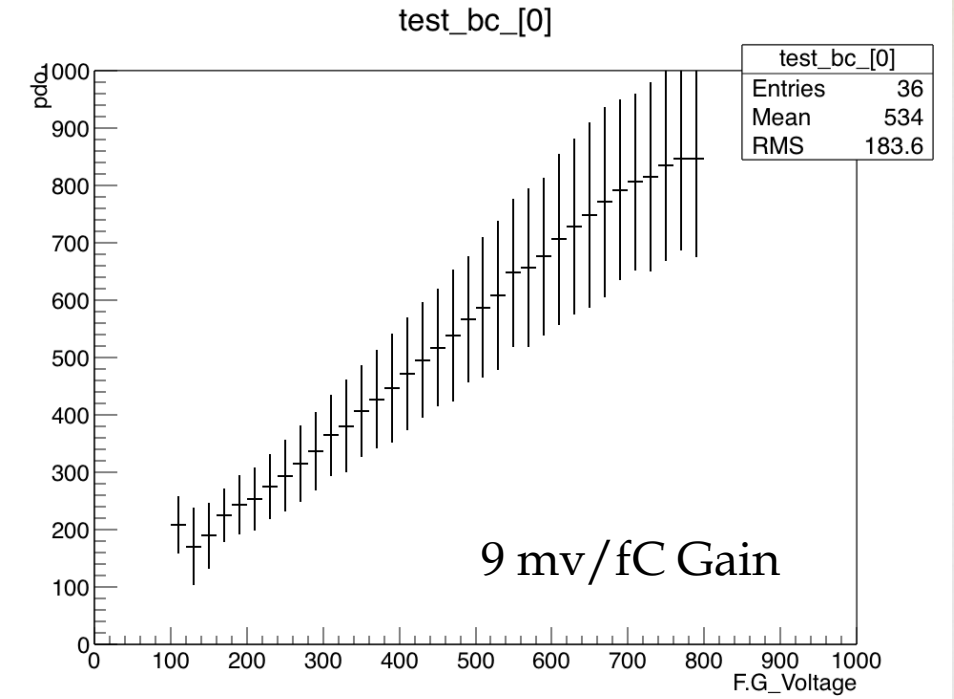


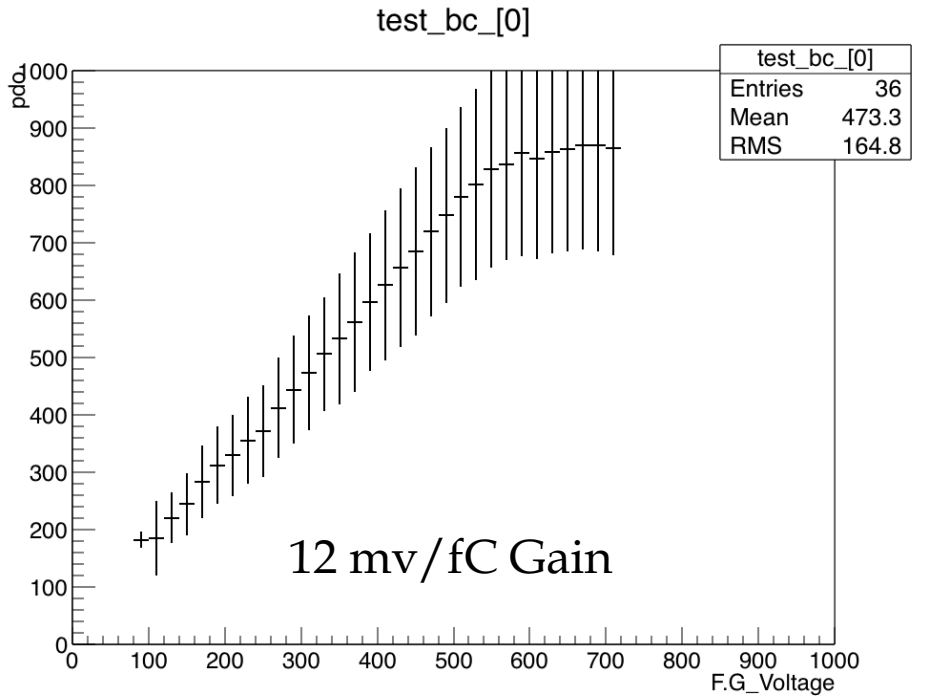
All channel test

128 ch pin + 2 GND pin

(130pin panasonic connector)



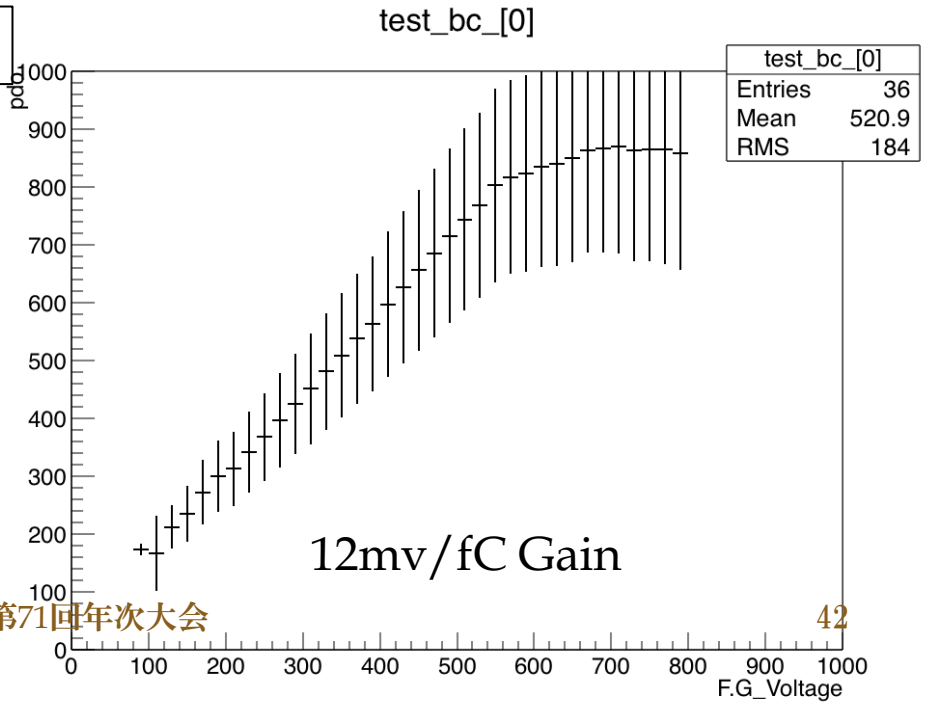




Data taking Condition

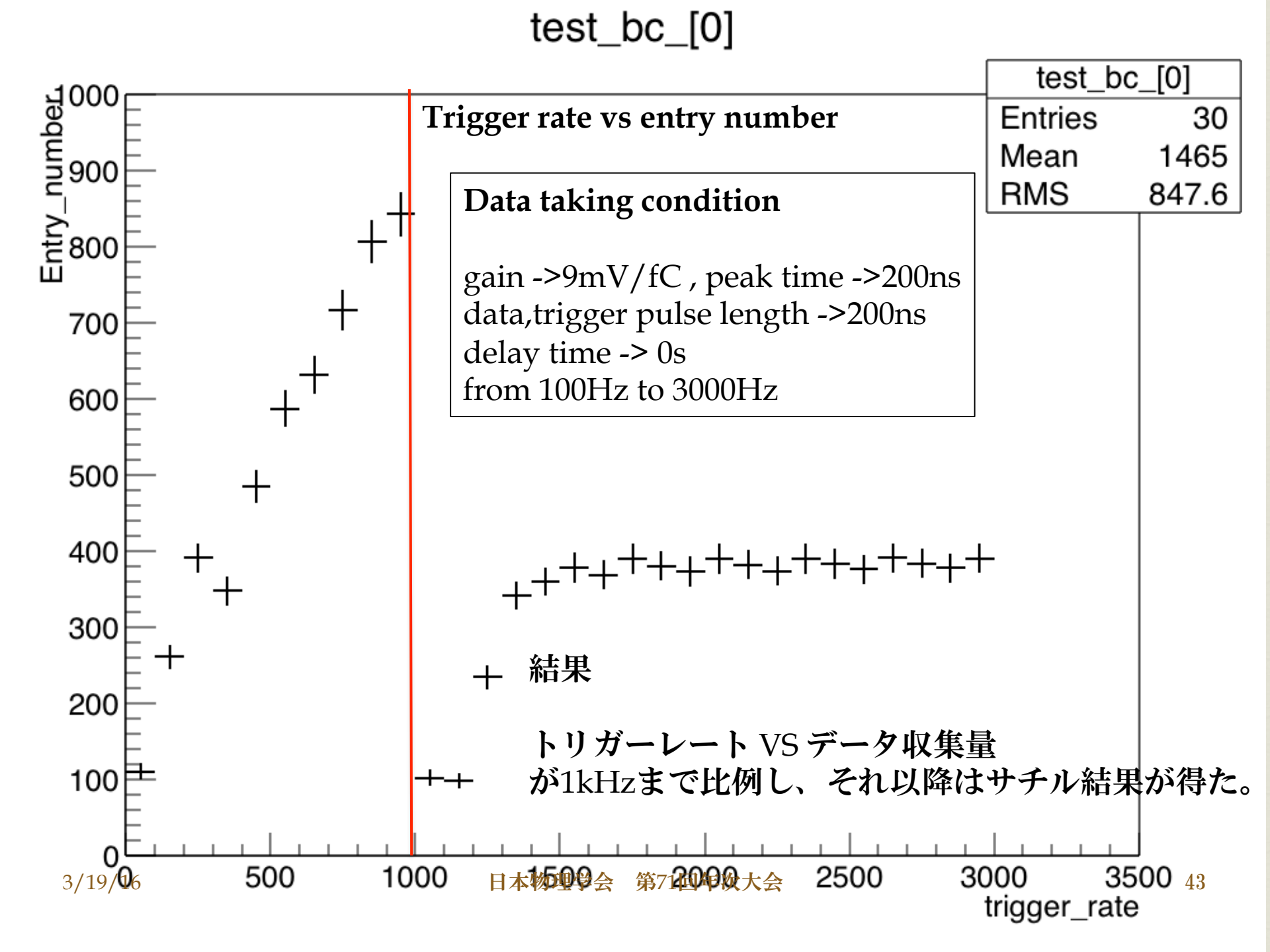
data trigger length 200ns
delay time 0s
trigger rate 2000Hz

F.G電圧 VS Pdo



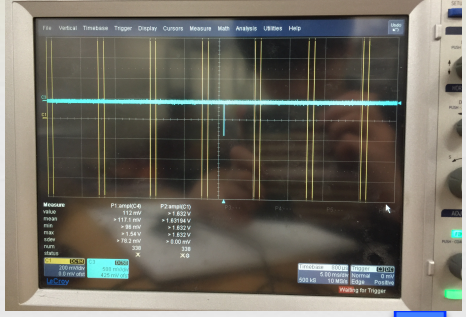
結果

- 各チャンネル毎にPdo値が違う
- GNDの方にも一緒に信号を送って結果、データに揺らぎが生じた


test_bc_[0]
Trigger rate vs entry number
test_bc_[0]
Entries 30
Mean 1465
RMS 847.6
Data taking condition
gain ->9mV/fC , peak time ->200ns
data,trigger pulse length ->200ns
delay time -> 0s
from 100Hz to 3000Hz
結果
トリガーレート VS データ収集量
が1kHzまで比例し、それ以降はサチル結果が得た。
Entry_number
trigger_rate
0
100
200
300
400
500
600
700
800
900
1000
500
1000
1500
2000
2500
3000
3500

External Signal test

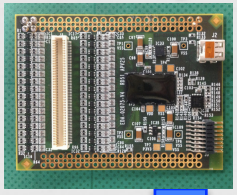
Function Generator
External trigger & external signal



Nim Cable

VMM2 chip

VMM2
Discriminator、shaper、
Peak & Time detector、
ADC(Analog Digital Converter)

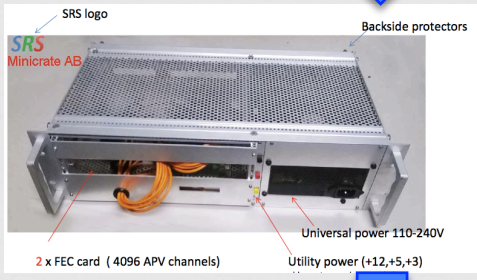


HDMI

SRS

SRS

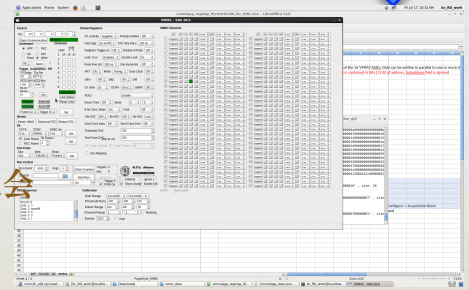
D-CARD
+FEC(Front End Concentrator)

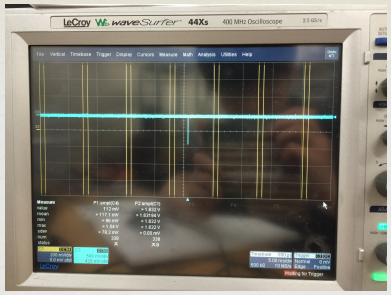


PC
NTU Athens

Ethernet

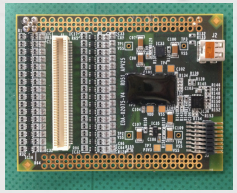
NTU Athens
Data taking & monitoring

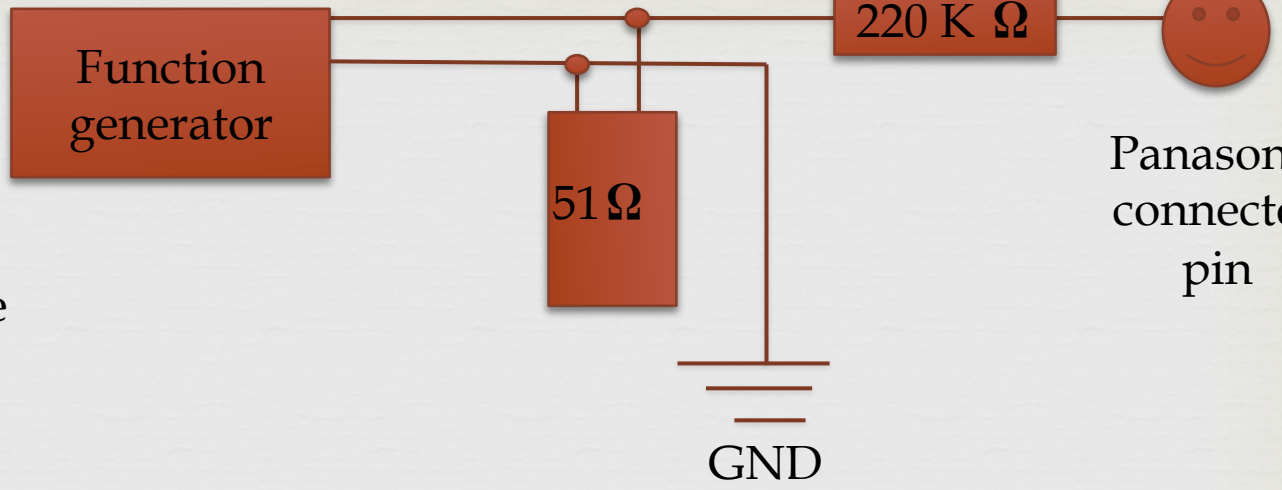




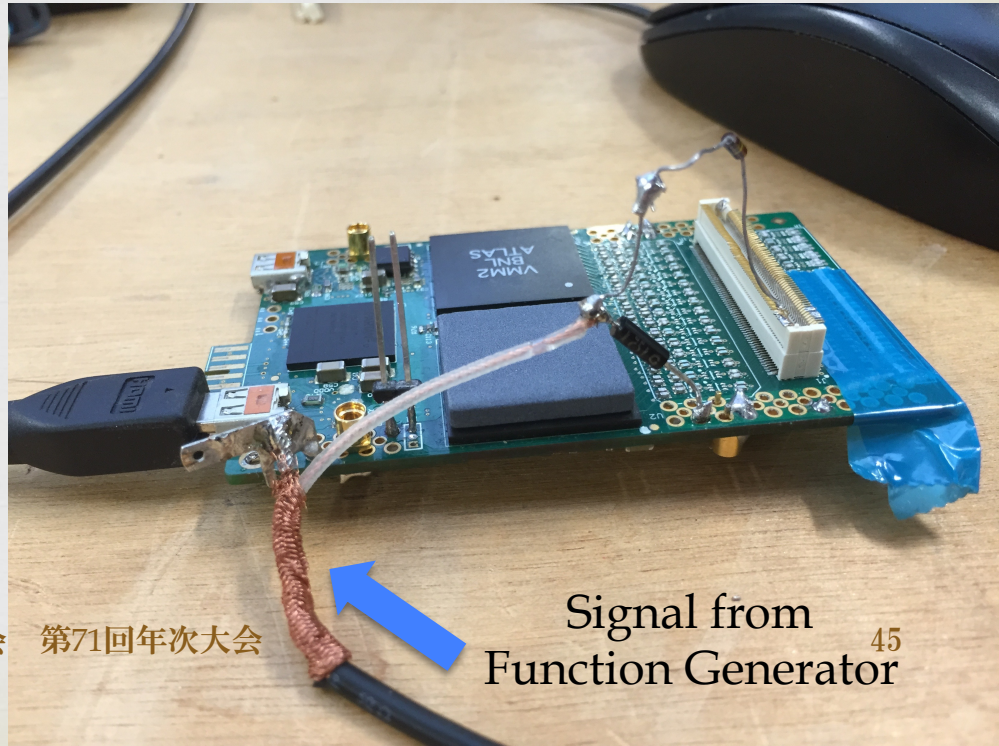
Nim Cable

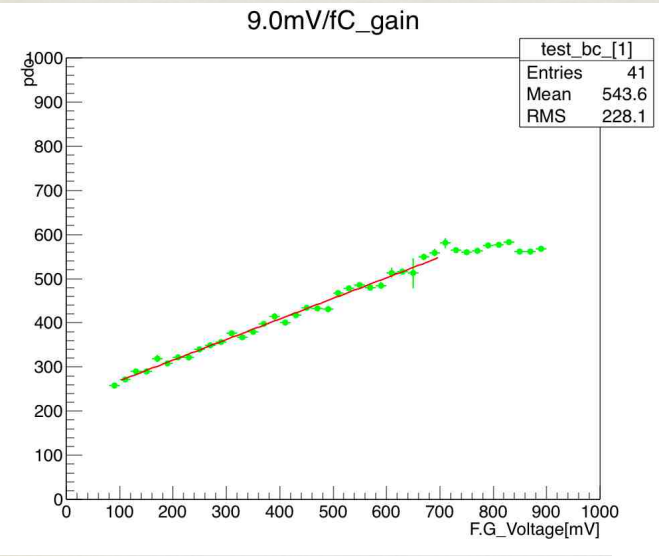
VMM2 chip

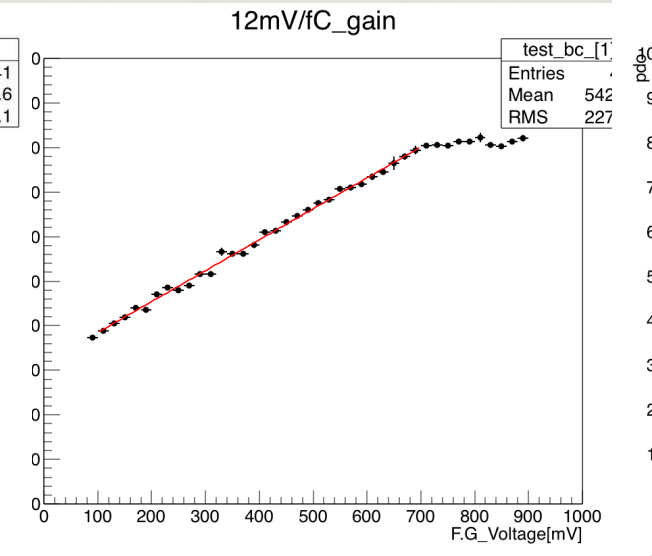


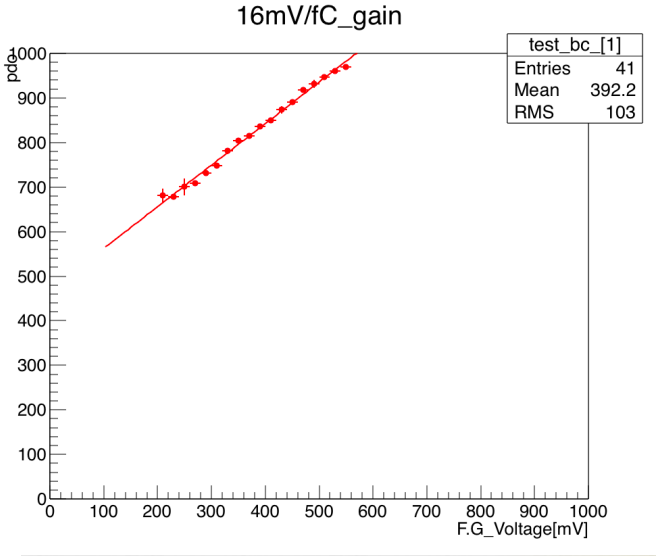


One channel test









Channel 58

Peak time 200ns