

ALICE FoCal-E PAD 検出器の信号読み出しに 向けたVMM2 チップの性能評価

Examining the SRS VMM2 based hybrid as a front-
end board for the ALICE FoCal-E Pad detector



University of Tsukuba, Tsukuba University of Technology^A,
CERN RD51 group^B

Byungchul Kim for the RD51 collaboration, Tatsuya Chujo, Motoi Inaba^A,
Hans Muller^B, George Iakovidis^B, Eraldo Oliveri^B

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Introduction

ALICE FoCal-E upgrade project at forward region(LHC long shutdown in 2020)

FoCal-E (Electro-magnetic calorimeter)

HGL(High Granularity Layer)

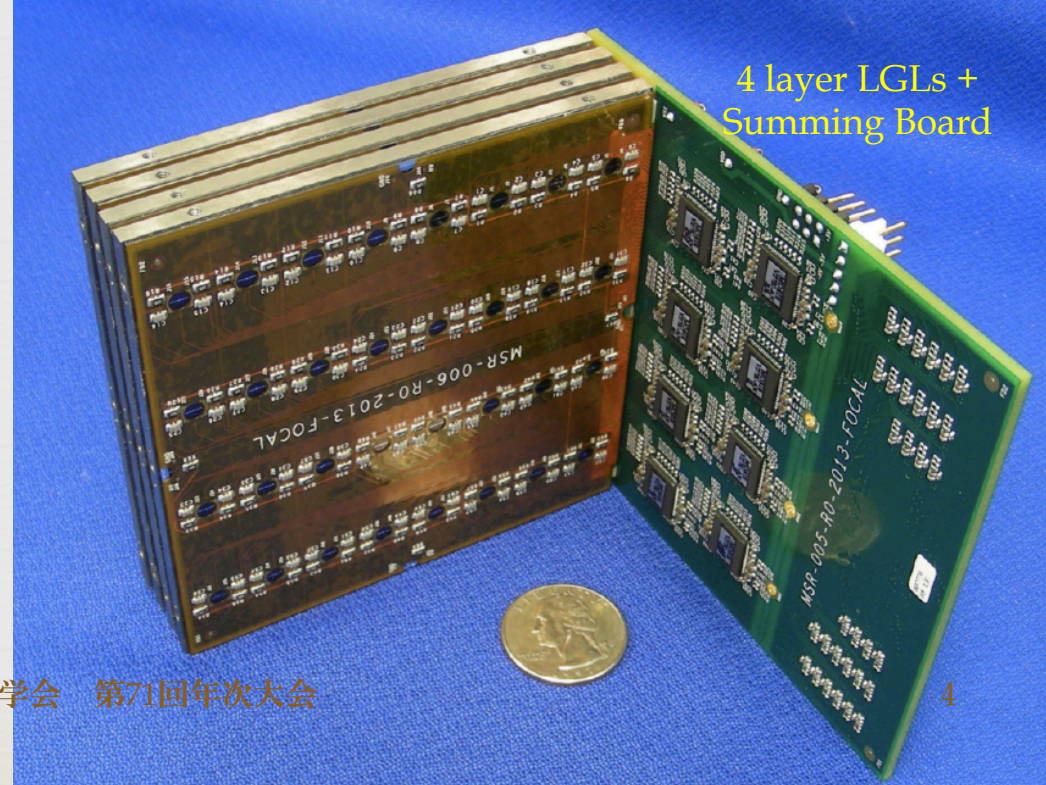
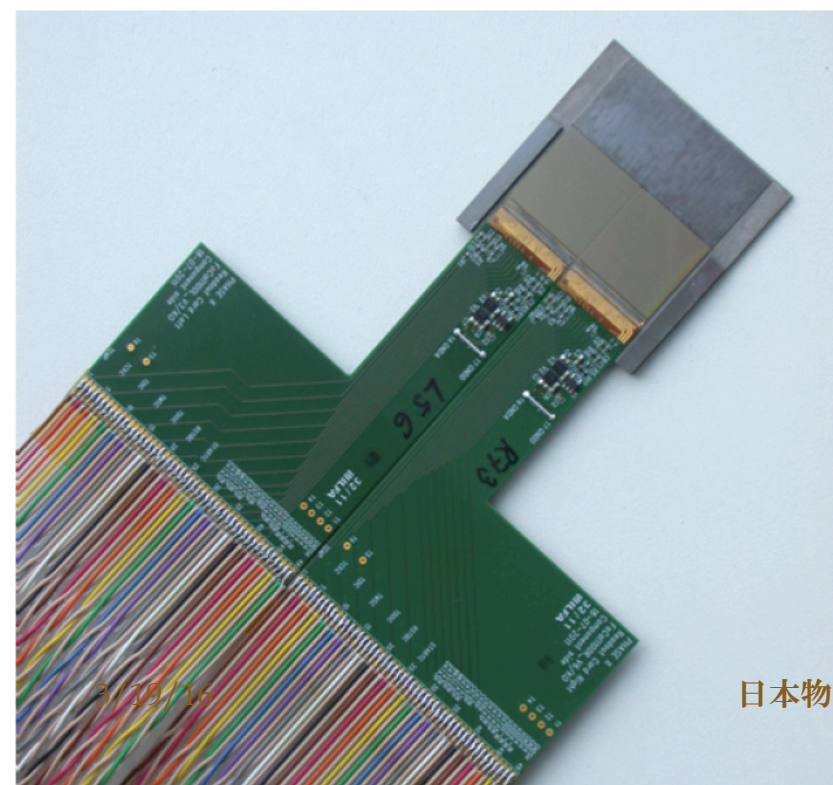
Shower position measurement
MAPS technology
(pixel $25 \mu\text{m}$)

Utrecht university(Nederland)

LGL(Low Granularity Layer)

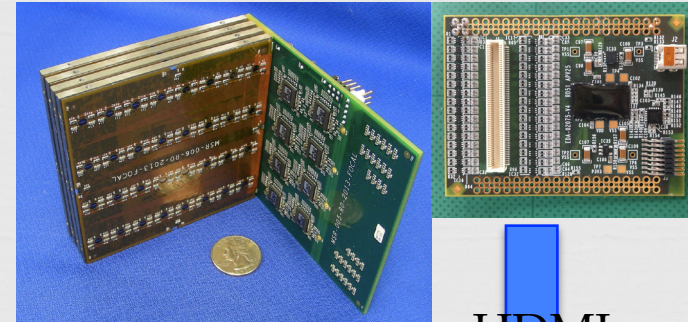
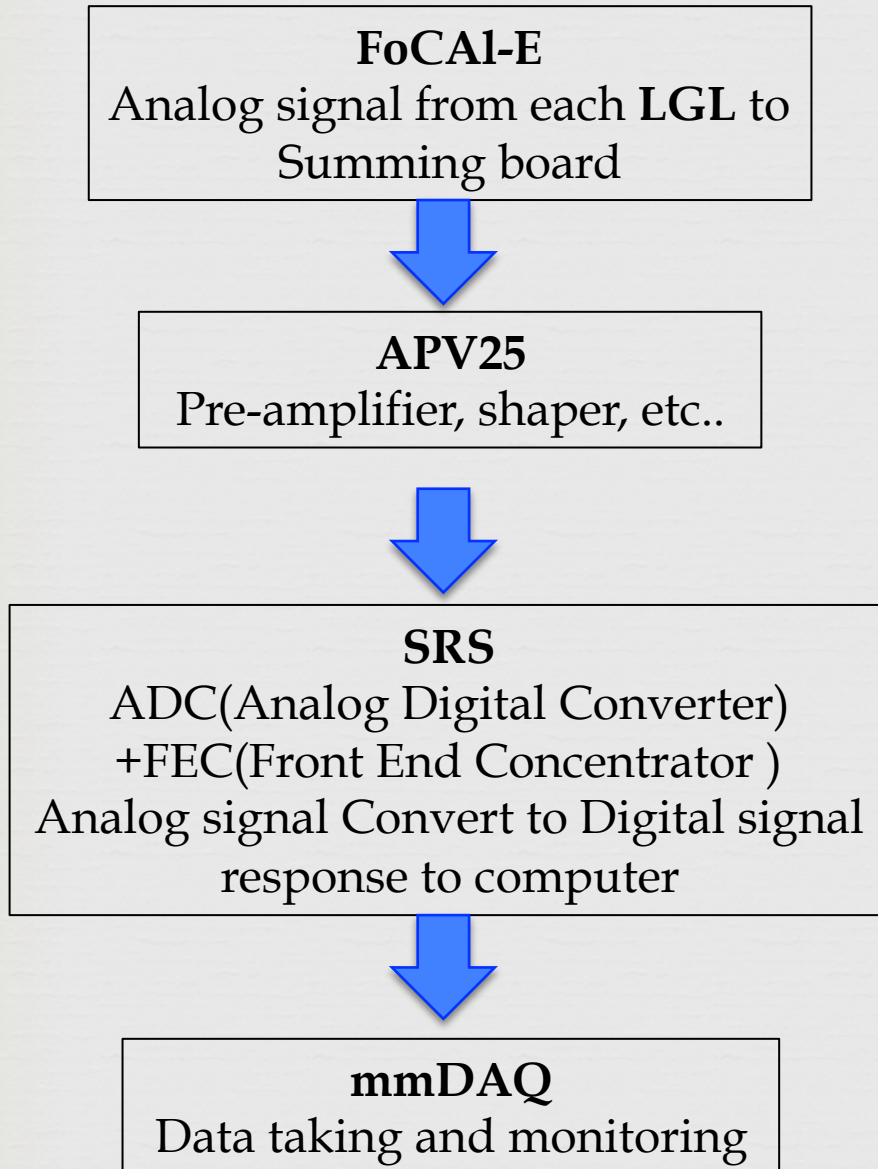
Photon shower energy measurement
Silicon PAD technology

Oak Ridge National Laboratory(U.S)
& University of Tsukuba



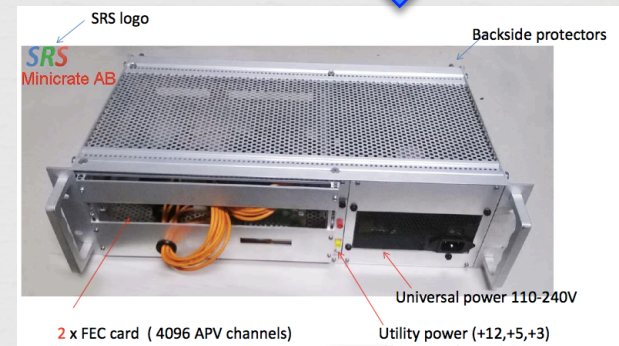
Current readout electronics system for FoCAI-E Pad

FoCal-E → APV25



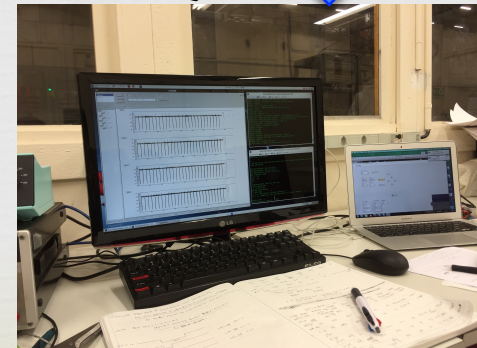
HDMI

SRS



PC
mmDAQ

Ethernet



Current problems of FoCAI-E pad and possible solution

1) Energy measurement is saturated near at 50GeV beam energy

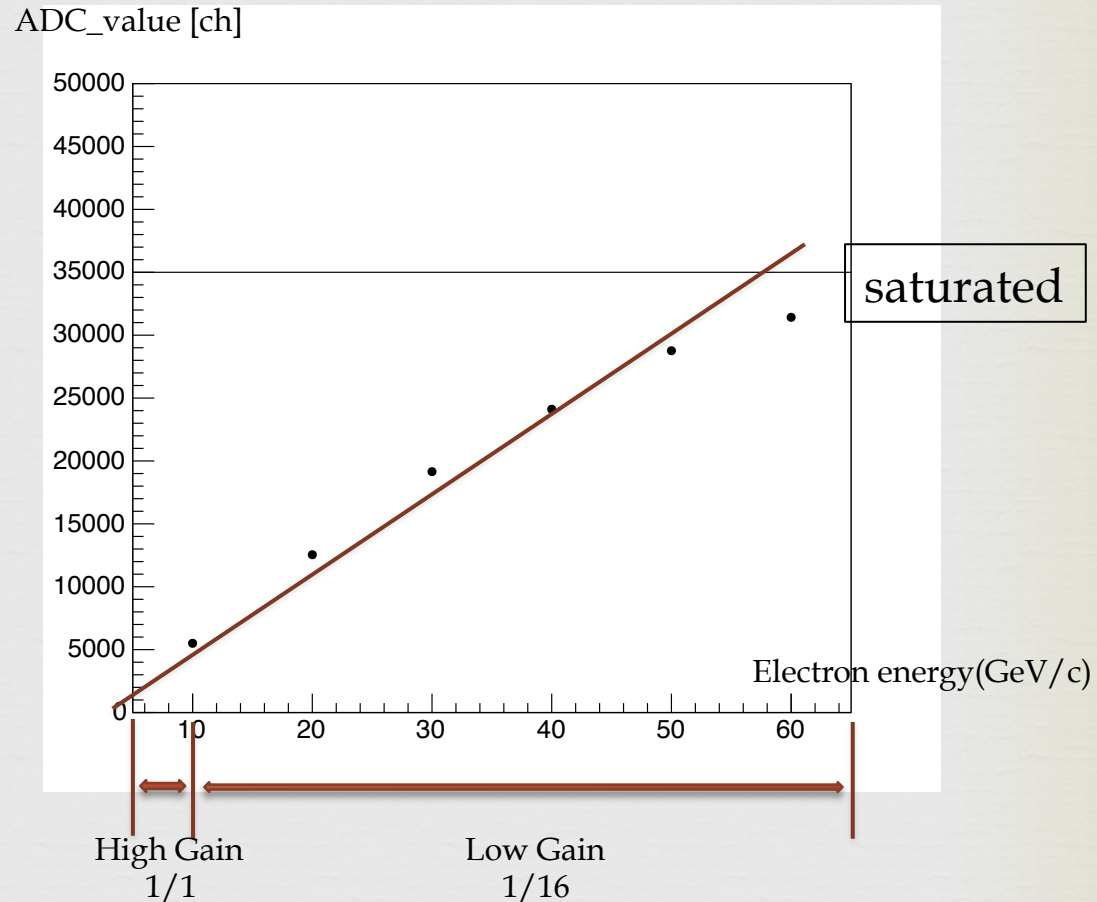


To meet our physics goal need more energy dynamic range up to 300GeV

2) Data taking rate with APV25 is 1kHz.



need faster data taking rate around 1MHz at forward region.

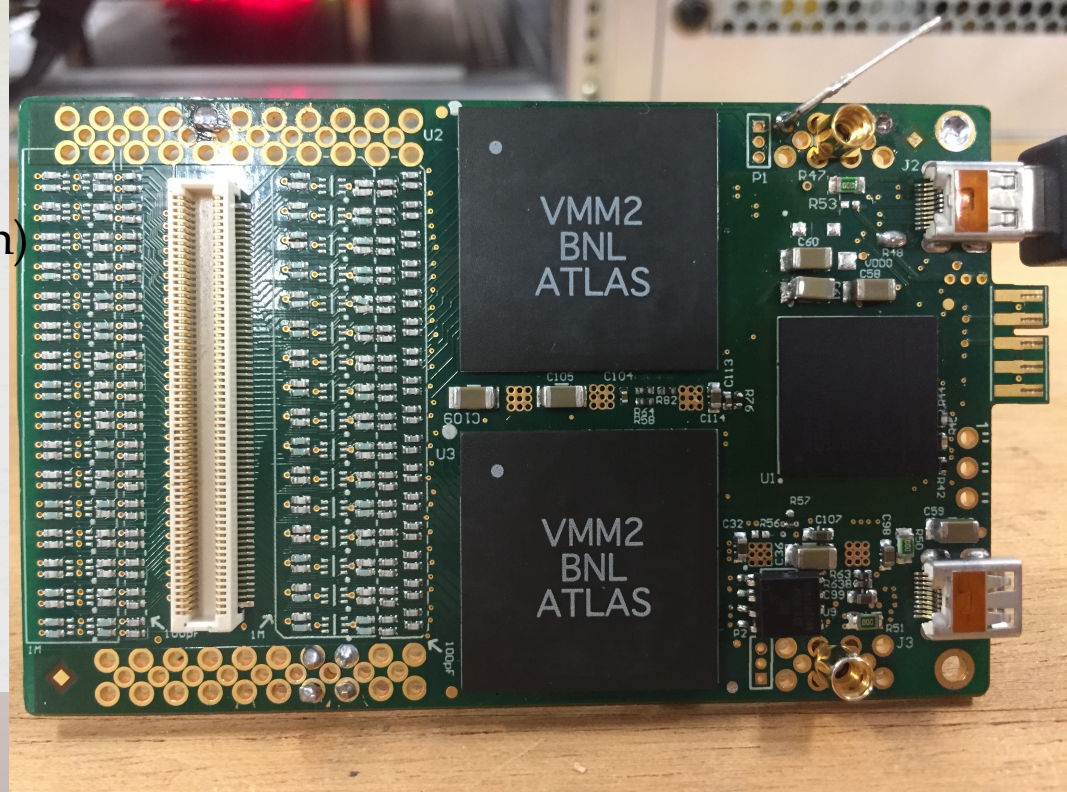


New readout system with VMM2 hybrid is tested with RD51 group.

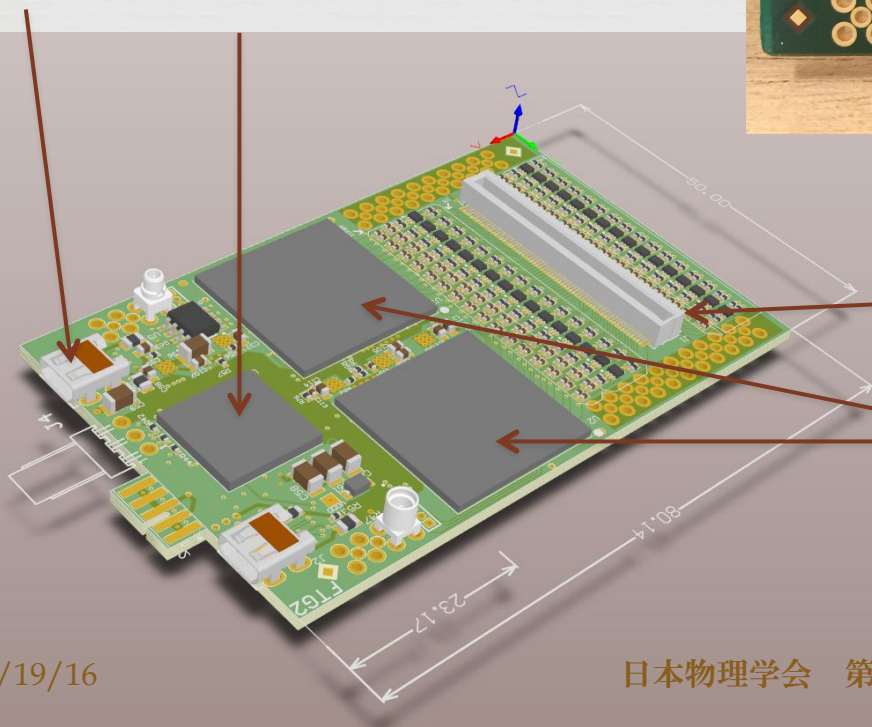
New readout system with VMM

VMM2 hybrid

- Standard Panasonic connector(130pin)
- 2 x VMM2 ASICs
- 1 x Spartan FPGA + 1 Flash
- 128 channel (64 x 2)
- readout rate could be 5MHz.



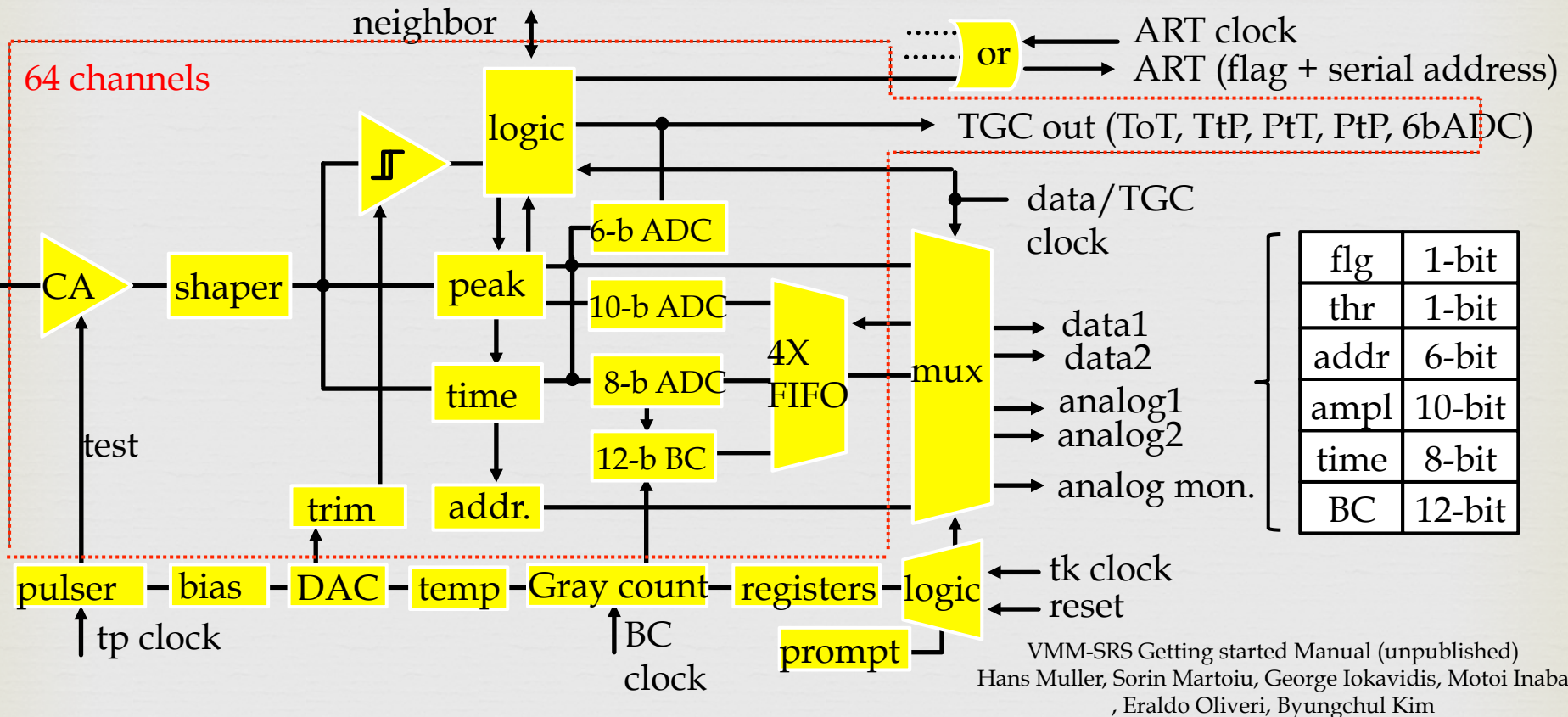
HDMI FPGA



Panasonic connector (130pin)

VMM2 ASIC

VMM2 Architecture - Complete ASIC



- VMM can get analog signal through shaper
- VMM has ADC(Analog Digital Converter) inside the chip
 - =>This function makes digital signal out put
 - =>It could be faster readout system compare to APV25 based SRS system with shorted ADC process
- VMM has internal test pulse

Readout system of VMM2 hybrid

VMM2
Discriminator, shaper,
ADC(Analog Digital Converter),etc..

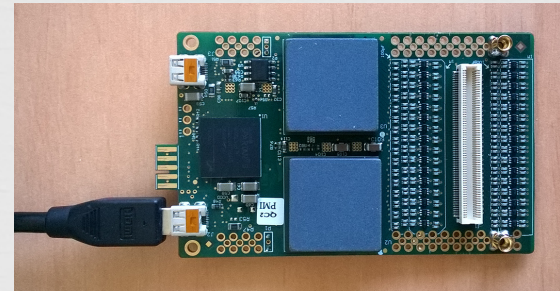


SRS
D-CARD
+FEC(Front End Concentrator)
Readout digital signal
Response to computer



NTU Athens(BNL)
Control VMM2 chips and take data

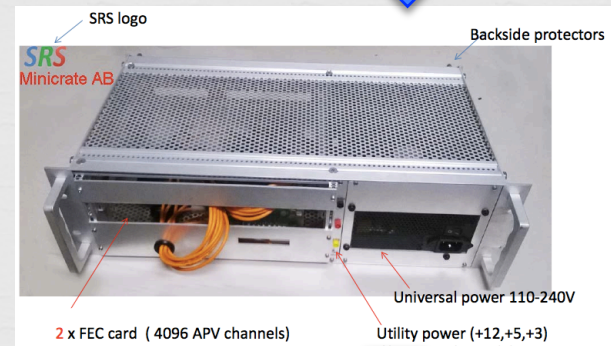
VMM2 hybrid



HDMI

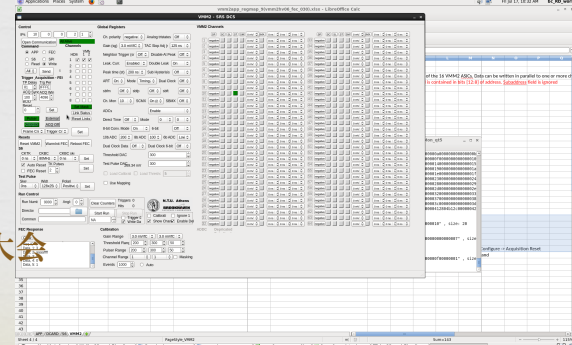


SRS



PC
NTU Athens

Ethernet



Analysis software

NTU Athens software – connect and control VMM2

The screenshot displays the NTU Athens software interface, which is used for connecting and controlling VMM2 channels. The interface is divided into several main sections:

- Control:** Contains IP address settings (10.0.0.2), communication status (All Alive), command options (APP, FEC, S6, SPI, Read, Write), trigger acquisition parameters (TP Delay, ACQ Sync, Trg Per, ACQ Win), and various control buttons like 'Pulser', 'External', 'ACQ On', and 'ACQ Off'.
- Global Registers:** A configuration panel for VMM2 channels with settings for polarity, gain, neighbor trigger, leak current, peak time, ART, sbfm, ch. mon, ADCs, direct time, 8-bit conv. mode, 10b ADC, dual clock data, threshold DAC, and test pulse DAC.
- VMM2 Channels:** A large grid showing the configuration for 64 channels. Each channel has a dropdown for polarity (e.g., negative) and several dropdowns for voltage (0 mV) and time (0 ns) settings.
- ADDC:** A section for ADC configuration with options for DAC, data, trigger, and counter, along with a time window setting.
- Run Control:** Includes run number (9003), angle (0), directory, and comments. It features 'Clear Counters', 'Start Run', and 'Stop Run' buttons, along with checkboxes for 'Calibration', 'Show Channels', and 'Enable Debug'.
- FEC Response:** A section for handling data reception, showing a 'Clear' button and a log of received data (e.g., 'Data Received Size: 24 bytes', 'Req ID: 7495').
- Calibration:** A section for setting calibration parameters, including gain range (3.0 mV/C), threshold range (200-300-50), pulser range (50-400-20), channel range (5-30), and events (1000).
- ADDC (Detailed):** A detailed view of the ADC configuration, including a 'Data Header' section with 'ACQ' and 'TAC Stop' settings, and a 'Trigger' section with 'Pulser', 'External', and 'Tr. Cnt' options.

Control

IPs 10 0 0 2 1

Open Communication Command **All Alive** Channels

APP FEC S6 SPI Read Write

Send 6

Trigger Acquisition - FE

TP Delay 81 Trg Per 3FFFE

ACQ Sync ACQ Win 100 4096

BCID

Reset 0

Pulser External

ACQ Off

Frame Cri Trigger Cri

Resets

Reset VMM2 WarmInit FEC Reboot FEC

S6

CKTK 0 ns CKBC 80MHz CKBC skt 0 ns

Auto Reset TK Pulses

FEC Reset 2

Test Pulse

Ske 0ns Wid 128x25 Polari Positive

Run Control

Run Numt 9000 Angl 0

Director

Comment 09/19/16

Clear Counters Triggers 0 Hits 0

Start Run Stop Run

NA

Calibrati Ignore 1

Write Da Show Chan Enable Def

Global Registers

Ch. polarity negative Analog tristates Off

Gain (sg) 3.0 mV/fC TAC Slop Adj (s 125 ns

Neighbor Trigger (sr Off Disable At Peak Off

Leak. Curr. Enabled Double Leak On

Peak time (st) 200 ns Sub Hysterisis Off

ART On Mode Timing Dual Clock Off

sbfm Off sbfp Off sbft Off

Ch. Mon 10 SCMX On (c SBMX Off

ADCs Enable

Direct Time Off Mode 0 0

8-bit Conv. Mode On 6-bit Off

10b ADC 200 8b ADC 100 6b ADC Low

Dual Clock Data Off Dual Clock 6-bit Off

Threshold DAC 300

Test Pulse DAC 269.34 mV 300

Load Calibrati Load Threshc 5

Use Mapping

Gain

It can select lots of gain as
0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC



It could take Wider energy
dynamic range

Peak time

It can select rise time Of signal
25, 50, 100, 200 ns

Monitoring channel

You can select channel
From 1 to 64 channel



N.T.U. Athens

BROOKHAVEN
NATIONAL LABORATORY

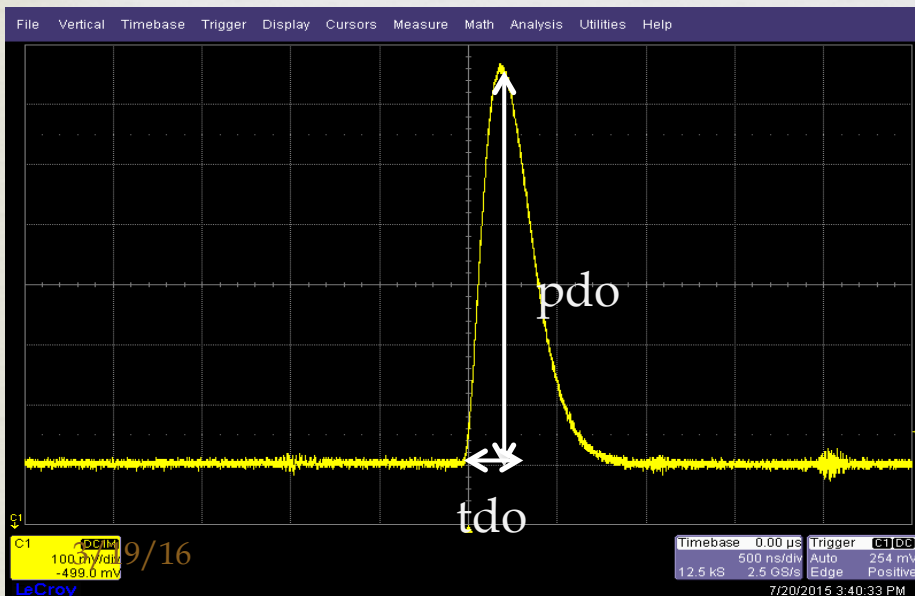
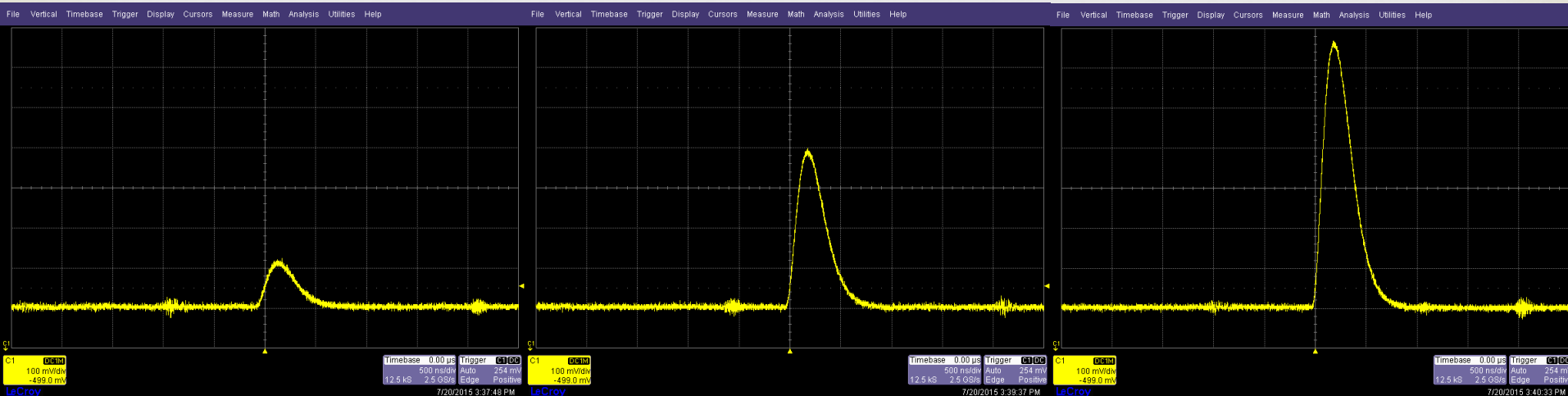
Results

Response check by internal Test Pulse DAC with oscilloscope

100 DAC

200 DAC

300 DAC



Pdo(peak detector output)

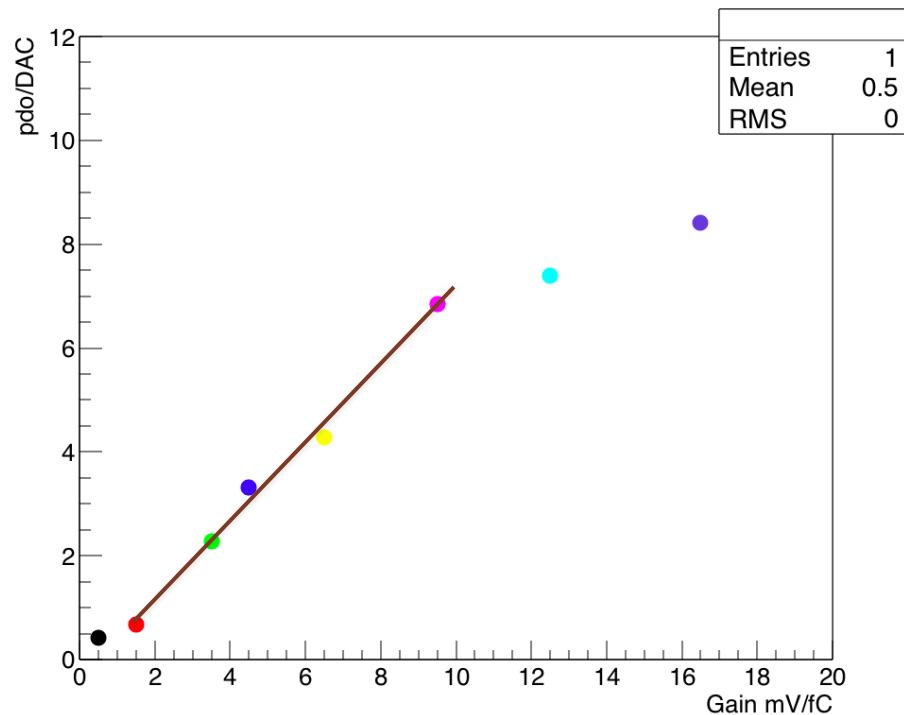
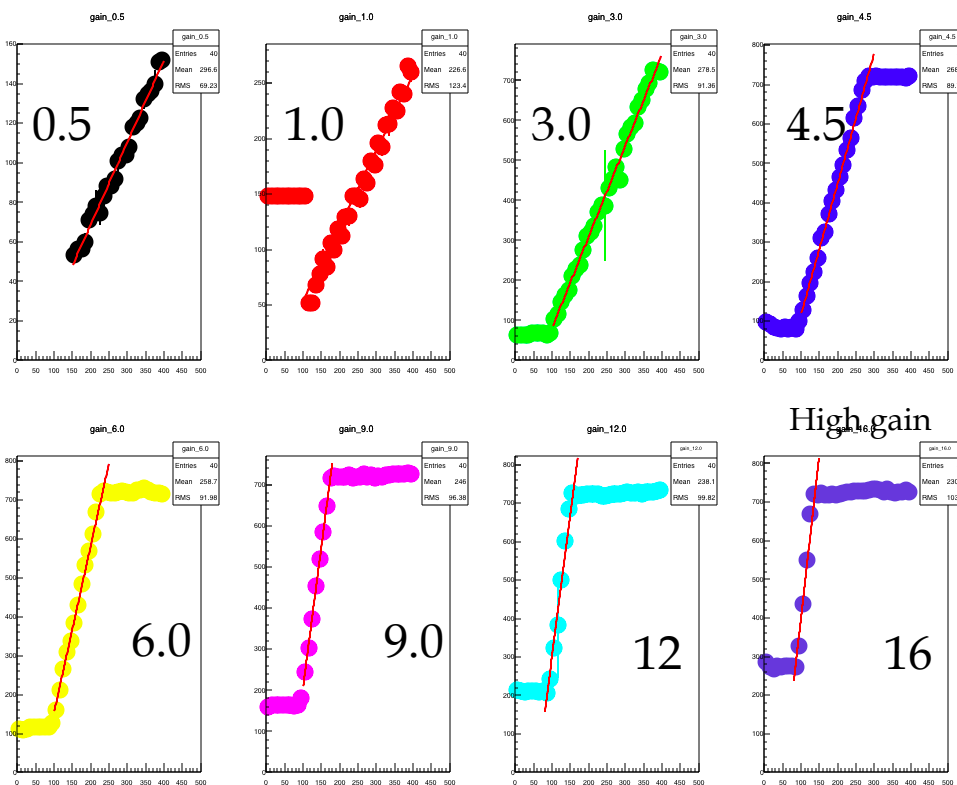
= return value of Amplitude

Tdo(time detector output)

= return value of Rise time

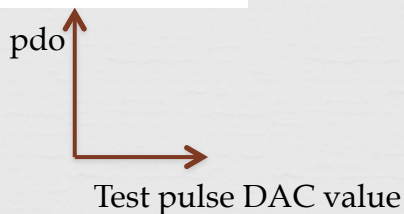
Linearity check with internal test pulse by gain variation

Low gain



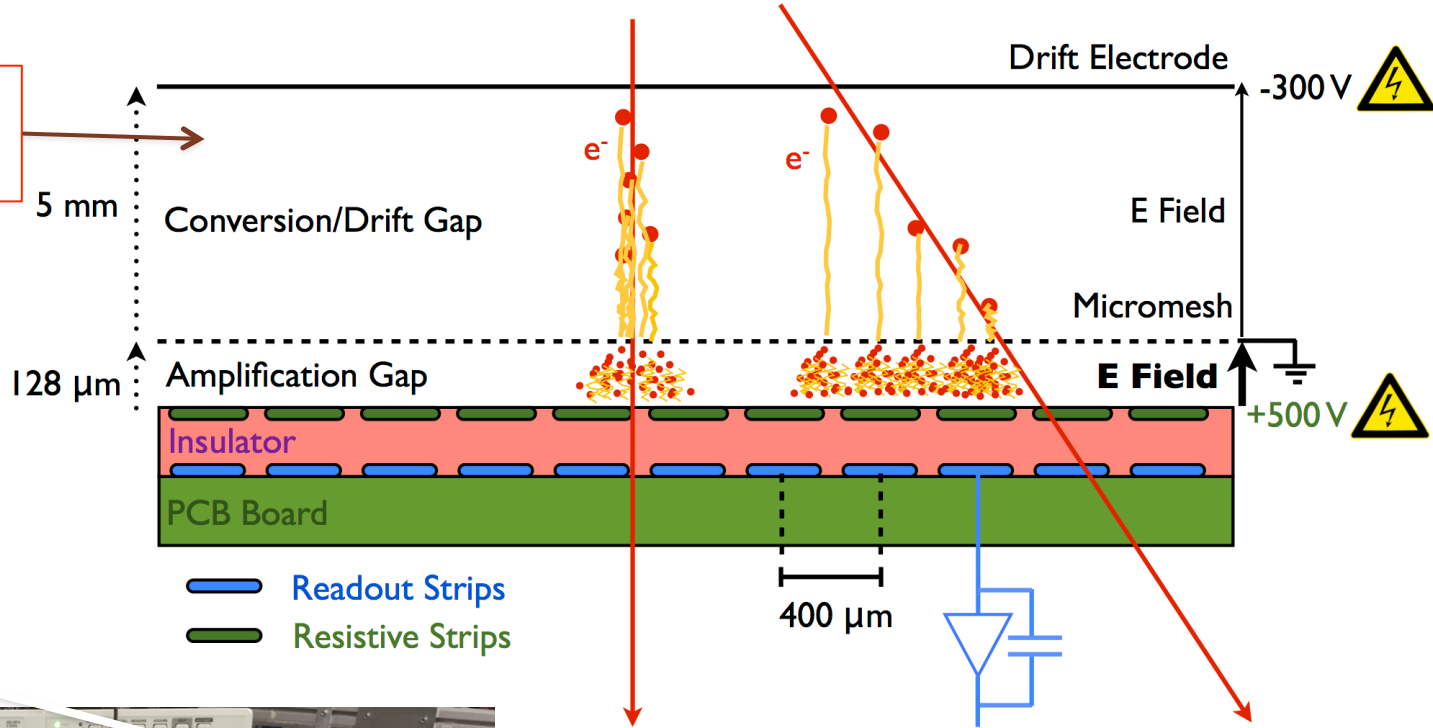
Gain 1.0 - 9.0 shows linearity.

Pdo vs Test pulse DAC value
Gain dependence
(0.5, 1.0, 3.0, 4.5, 6.0, 9.0, 12, 16)

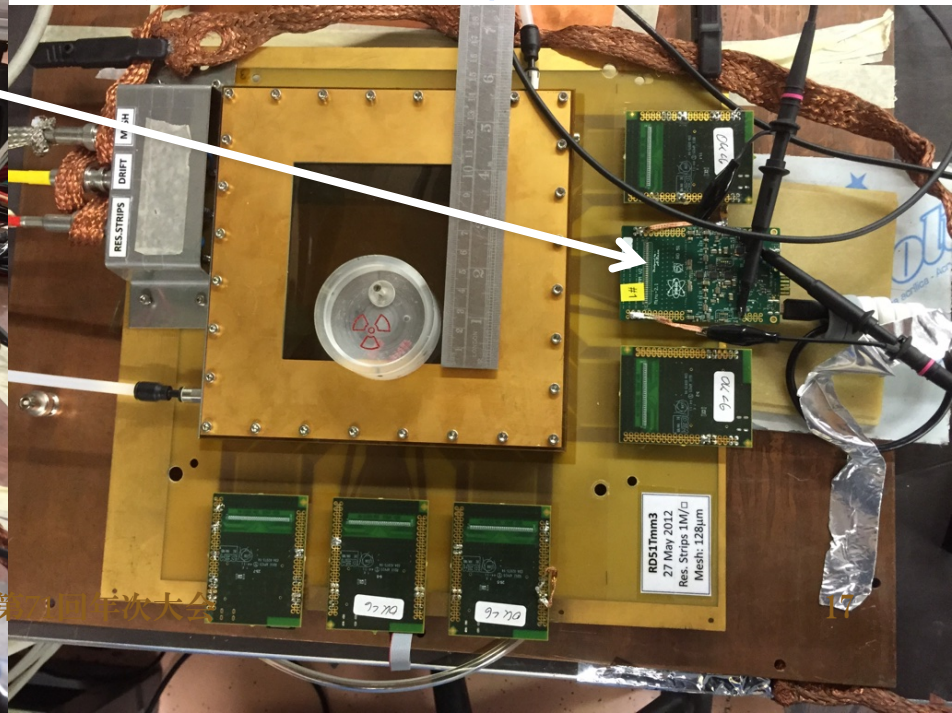
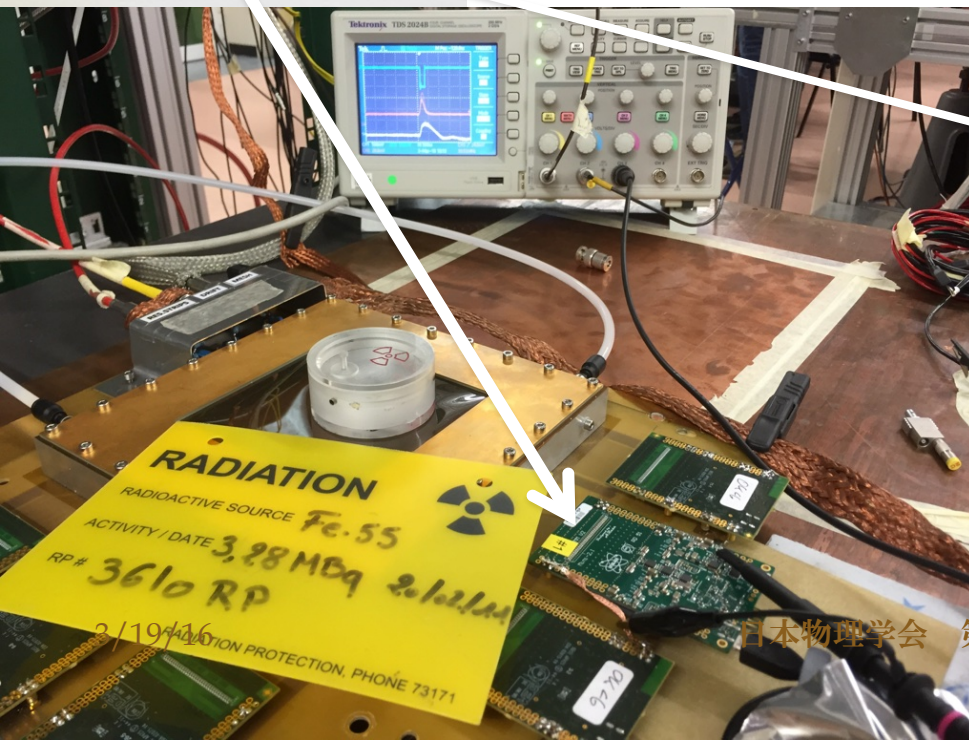


VMM test with Micro Megas

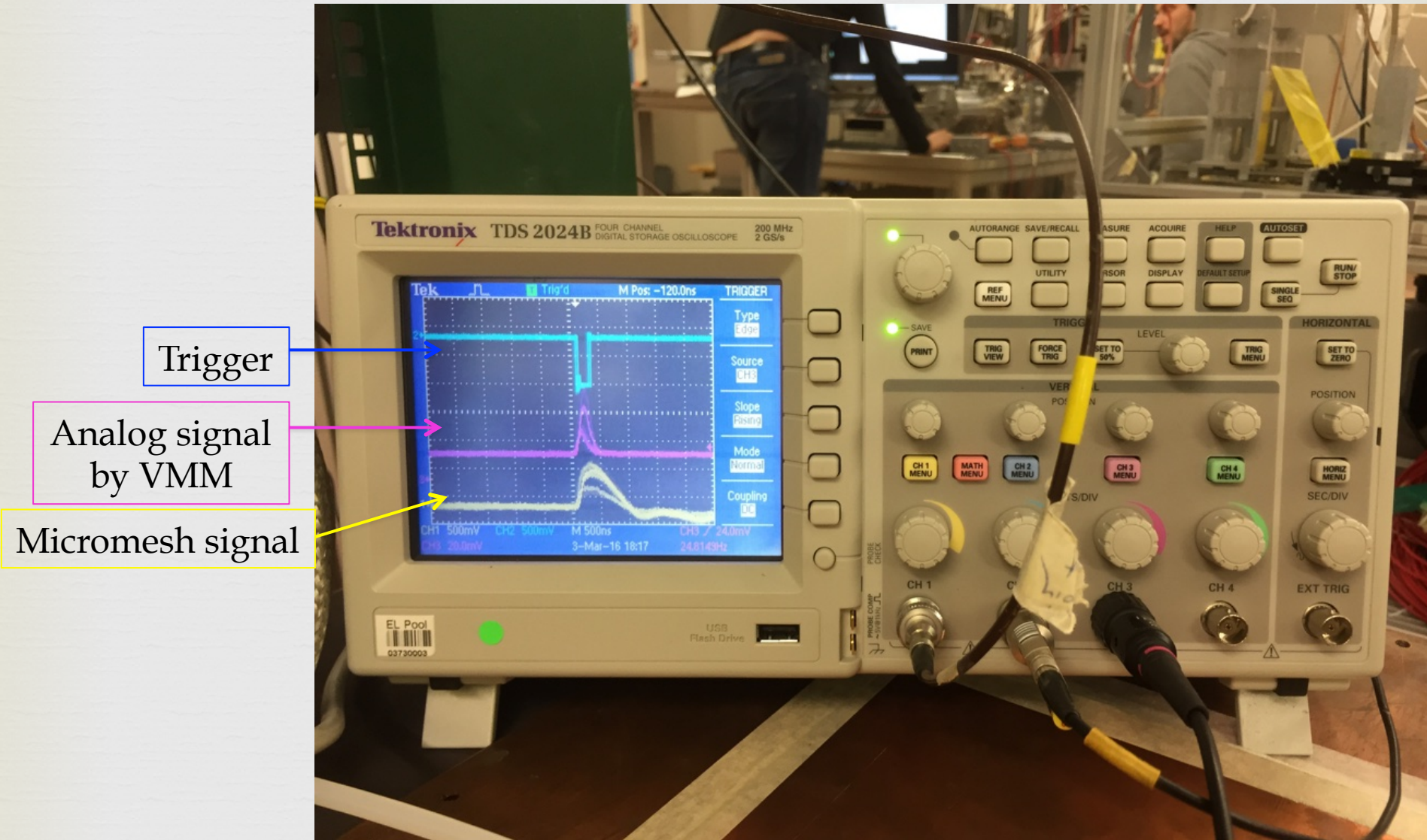
Gas electric field



VMM2 hybrid



VMM2 Response check With Micro Megas detector



Summary & out look

Summary

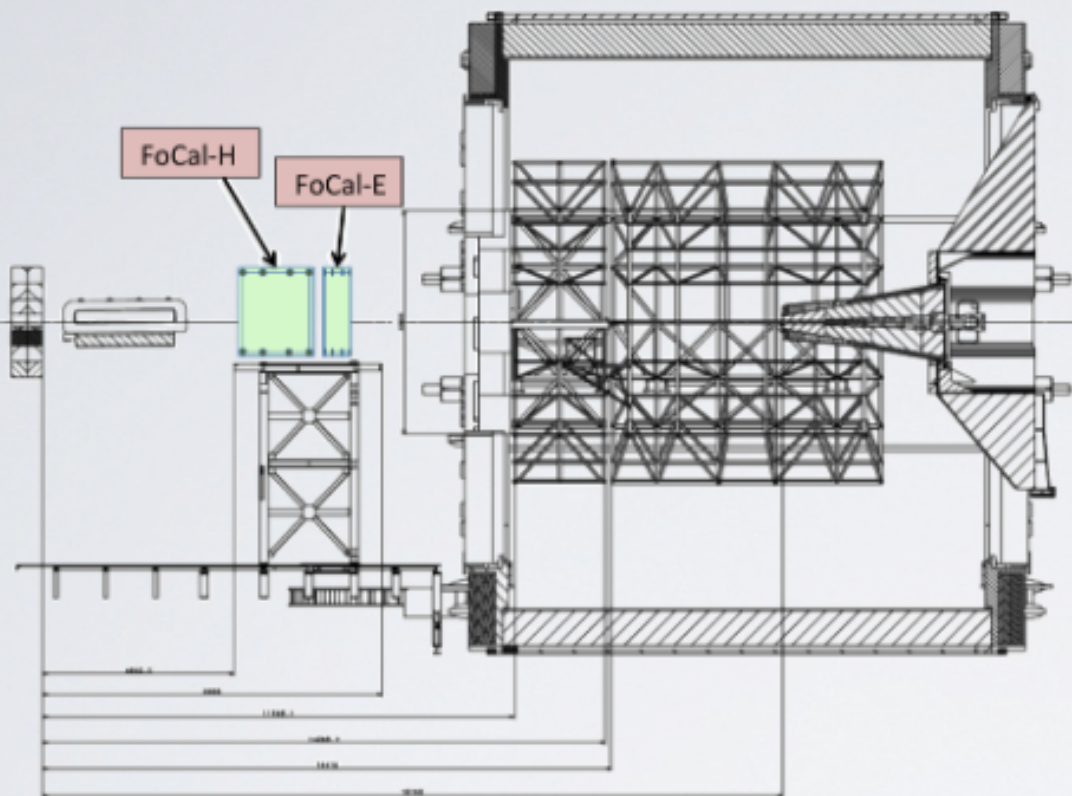
- Development & Research of new readout for FoCA1 - E pad
- Built a test bench for VMM2 hybrid at RD51 lab
- Checked VMM2 hybrid response with internal , external pulse
- Tested VMM2 hybrid with Micro Megas detector

Out look

- development new software for test higher speed readout.
- VMM3(next version of VMM2) will be produced and tested as a new readout system.
- New LGL summing board toward VMM will be developed.
- Beam test will be conducted for FoCA1-E with VMM hybrid.

Back up

ALICE Upgrade Project - FoCal detector (toward LHC long shutdown at 2020 years)



- location of installation
 - 7m at z direction from collision point.
- acceptance
 - $3.3 < \eta < 5.3$
- structure
 - electro-magnetic calorimeter (FoCal-E)
 - hadron calorimeter (FoCal-H)
- purpose
 - To Detect jet effect and direct photon at forward.

FoCal-E

Z=7 m

$\eta = 5.3$

$\eta = 3.3$

θ



For IP Connection

(ping status 10.0.0.2)

Sending internal analog signal within VMM2

Start acquisition

Decide root name and directory

3/19/16

Control

IPs 10 0 0 2 1

Open Communication Command **All Alive** Channels

APP FEC
 S6 SPI
 Read Write

	HDM	VMM2
	1	2
1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
2	<input type="checkbox"/>	<input type="checkbox"/>
3	<input type="checkbox"/>	<input type="checkbox"/>
4	<input type="checkbox"/>	<input type="checkbox"/>
5	<input type="checkbox"/>	<input type="checkbox"/>
6	<input type="checkbox"/>	<input type="checkbox"/>
7	<input type="checkbox"/>	<input type="checkbox"/>
8	<input type="checkbox"/>	<input type="checkbox"/>

Resets

S6

CKTK 0 ns CKBC 80MHz CKBC ski 0 ns

Auto Reset FEC Reset

Test Pulse

Sker 0ns Widr 128x25i Polari Positive

Run Control

Run Numt 9000 Angl 0

Director

Commen

Trigger E Write Da

Global Registers

Ch. polarity negative Analog tristates Off

Gain (sg) 3.0 mV/fC TAC Slop Adj (s) 125 ns

Neighbor Trigger (sr) Off Disable At Peak Off

Leak. Curr. Enabled Double Leak On

Peak time (st) 200 ns Sub Hysterisis Off

ART On Mode Timing Dual Clock Off

sbfm Off sbfp Off sbft Off

Ch. Mon 10 SCMX On (c) SBMX Off

ADCs Enable

Direct Time Off Mode 0 0

8-bit Conv. Mode On 6-bit Off

10b ADC 200 8b ADC 100 6b ADC Low

Dual Clock Data Off Dual Clock 6-bit Off

Threshold DAC 300

269.34 mV 300

Load Calibrati Load Threshc 5

Use Mapping

Triggers 0
 Hits 0

Calibrati Ignore 1
 Show Char Enable Del

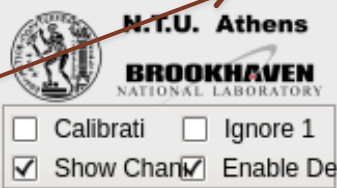
Gain, Peak time, Monitoring Channel, etc..

Control internal test pulser DAC

Start to make root file

Close to make root file

日本物理学会 第71回年次大会



VMM2 Channels

	SP	SC	SL	ST	SM	0 mV	SMX	0 ns	0 ns	0 ns		SP	SC	SL	ST	SM	0 mV	SMX	0 ns	0 ns	0 ns	
1	negative					0 mV		0 ns	0 ns	0 ns		33	negative				0 mV		0 ns	0 ns	0 ns	
2	negative					0 mV		0 ns	0 ns	0 ns		34	negative				0 mV		0 ns	0 ns	0 ns	
3	negative					0 mV		0 ns	0 ns	0 ns		35	negative				0 mV		0 ns	0 ns	0 ns	
4	negative					0 mV		0 ns	0 ns	0 ns		36	negative				0 mV		0 ns	0 ns	0 ns	
5	negative					0 mV		0 ns	0 ns	0 ns		37	negative				0 mV		0 ns	0 ns	0 ns	
6	negative					0 mV		0 ns	0 ns	0 ns		38	negative				0 mV		0 ns	0 ns	0 ns	
7	negative					0 mV		0 ns	0 ns	0 ns		39	negative				0 mV		0 ns	0 ns	0 ns	
8	negative					0 mV		0 ns	0 ns	0 ns		40	negative				0 mV		0 ns	0 ns	0 ns	
9	negative					0 mV		0 ns	0 ns	0 ns		41	negative				0 mV		0 ns	0 ns	0 ns	
10	negative					0 mV		0 ns	0 ns	0 ns		42	negative				0 mV		0 ns	0 ns	0 ns	
11	negative					0 mV		0 ns	0 ns	0 ns		43	negative				0 mV		0 ns	0 ns	0 ns	
12	negative					0 mV		0 ns	0 ns	0 ns		44	negative				0 mV		0 ns	0 ns	0 ns	
13	negative					0 mV		0 ns	0 ns	0 ns		45	negative				0 mV		0 ns	0 ns	0 ns	
14	negative					0 mV		0 ns	0 ns	0 ns		46	negative				0 mV		0 ns	0 ns	0 ns	
15	negative					0 mV		0 ns	0 ns	0 ns		47	negative				0 mV		0 ns	0 ns	0 ns	
16	negative					0 mV		0 ns	0 ns	0 ns		48	negative				0 mV		0 ns	0 ns	0 ns	
17	negative					0 mV		0 ns	0 ns	0 ns		49	negative				0 mV		0 ns	0 ns	0 ns	
18	negative					0 mV		0 ns	0 ns	0 ns		50	negative				0 mV		0 ns	0 ns	0 ns	
19	negative					0 mV		0 ns	0 ns	0 ns		51	negative				0 mV		0 ns	0 ns	0 ns	
20	negative					0 mV		0 ns	0 ns	0 ns		52	negative				0 mV		0 ns	0 ns	0 ns	
21	negative					0 mV		0 ns	0 ns	0 ns		53	negative				0 mV		0 ns	0 ns	0 ns	
22	negative					0 mV		0 ns	0 ns	0 ns		54	negative				0 mV		0 ns	0 ns	0 ns	
23	negative					0 mV		0 ns	0 ns	0 ns		55	negative				0 mV		0 ns	0 ns	0 ns	
24	negative					0 mV		0 ns	0 ns	0 ns		56	negative				0 mV		0 ns	0 ns	0 ns	
25	negative					0 mV		0 ns	0 ns	0 ns		57	negative				0 mV		0 ns	0 ns	0 ns	
26	negative					0 mV		0 ns	0 ns	0 ns		58	negative				0 mV		0 ns	0 ns	0 ns	
27	negative					0 mV		0 ns	0 ns	0 ns		59	negative				0 mV		0 ns	0 ns	0 ns	
28	negative					0 mV		0 ns	0 ns	0 ns		60	negative				0 mV		0 ns	0 ns	0 ns	
29	negative					0 mV		0 ns	0 ns	0 ns		61	negative				0 mV		0 ns	0 ns	0 ns	
30	negative					0 mV		0 ns	0 ns	0 ns		62	negative				0 mV		0 ns	0 ns	0 ns	
31	negative					0 mV		0 ns	0 ns	0 ns		63	negative				0 mV		0 ns	0 ns	0 ns	
32	negative					0 mV		0 ns	0 ns	0 ns		64	negative				0 mV		0 ns	0 ns	0 ns	

64channels

Can be controlled

SP=adjustable polarity

SC=Sensor Capacitance

SL=Leakage Current disable

ST=1.2pF, Test Capacitor enable

SM=Mask enable

Run Control

Run Numt: 9000 Angl: 0 Clear Counters Triggers 0 Hits 0

Director: [Folder Icon] Start Run Stop Run

Commen: [Text Field] NA Trigger E Calibrati Ignore 1

Write Da Show Chan Enable Del

FEC Response

Clear

Req ID :6
Data, 1: 3
Data, 2: aaaaffff
Data, 3: 0
Data, 4: 0
Data, 5: 1

Calibration

Gain Range: 3.0 mV/fC 3.0 mV/fC

Threshold Rang: 200 300 50

Pulser Range: 200 300 50

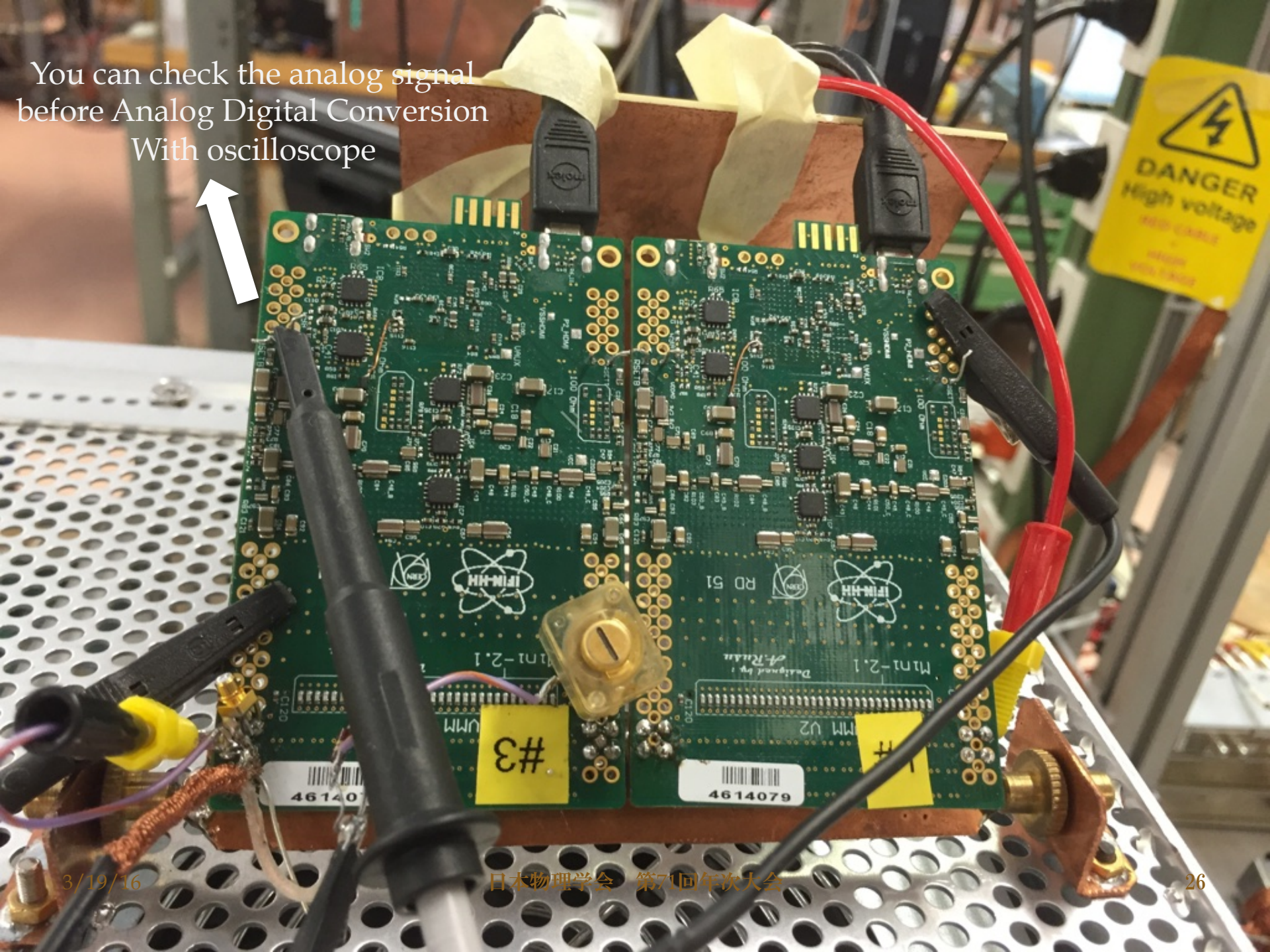
Channel Range: 1 1 Masking

Events: 1000 Auto

Calibration => It can make macros with internal test pulse.
Gain, Pulse range, channels, Number of Events

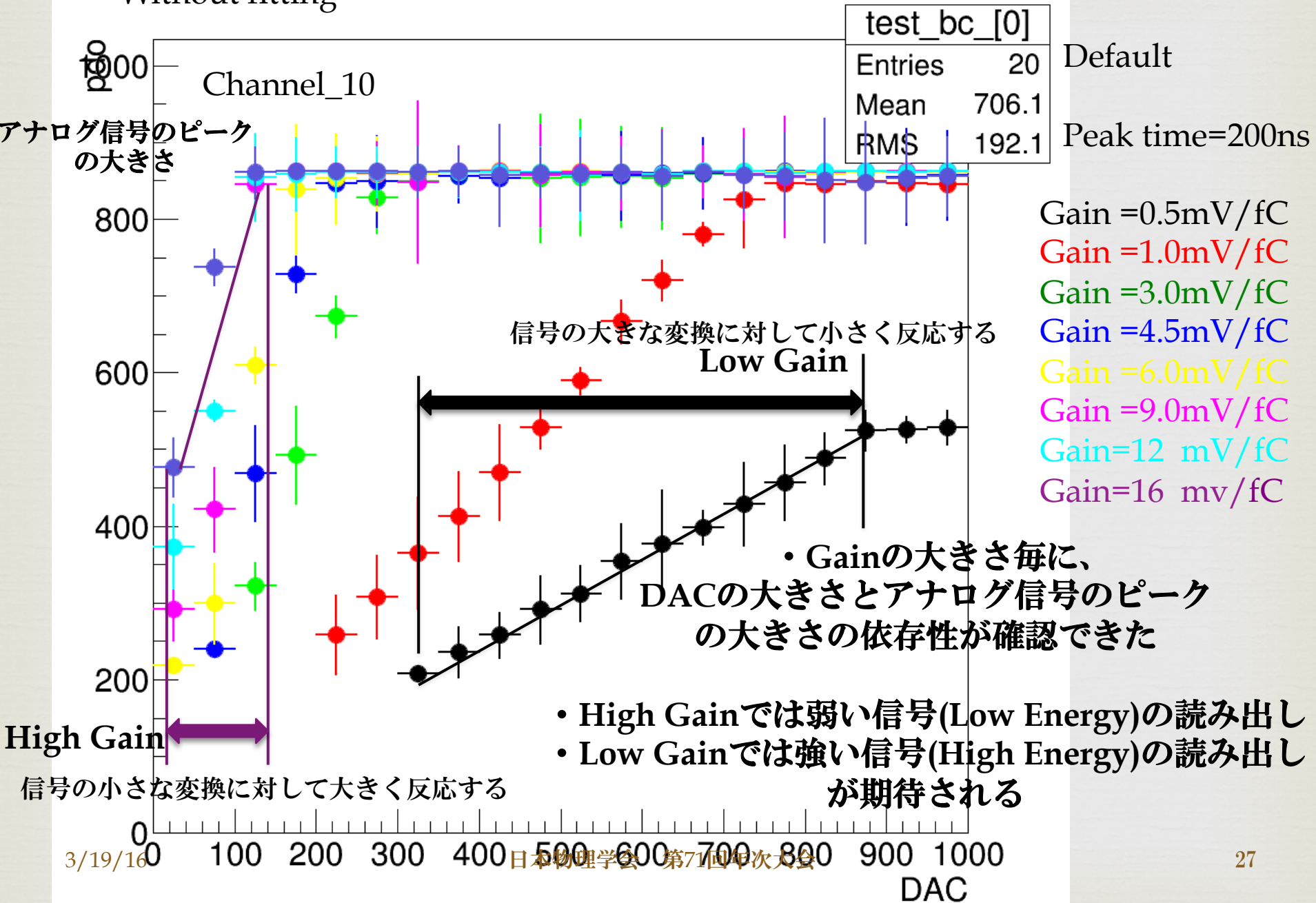
Trigger Data => to observe response of VMM2 with external trigger

You can check the analog signal before Analog Digital Conversion
With oscilloscope



test_bc_[0]

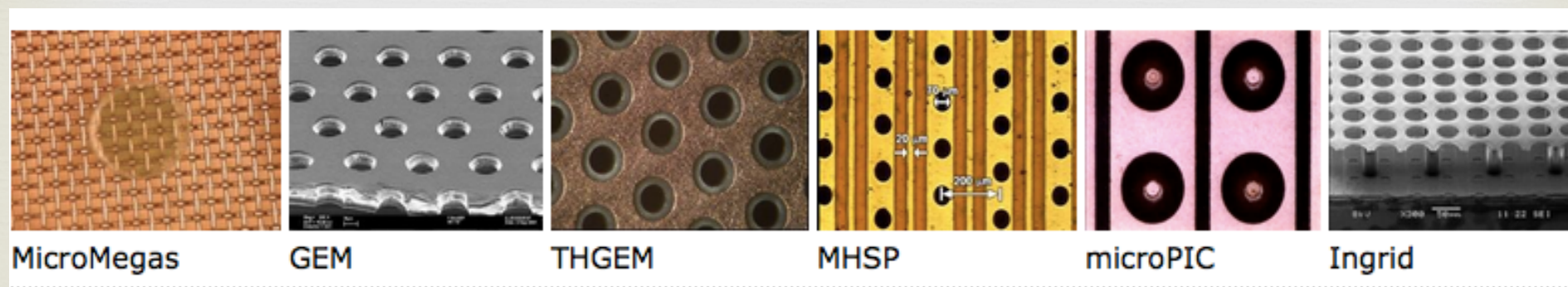
Without fitting



RD51 Collaborationの紹介

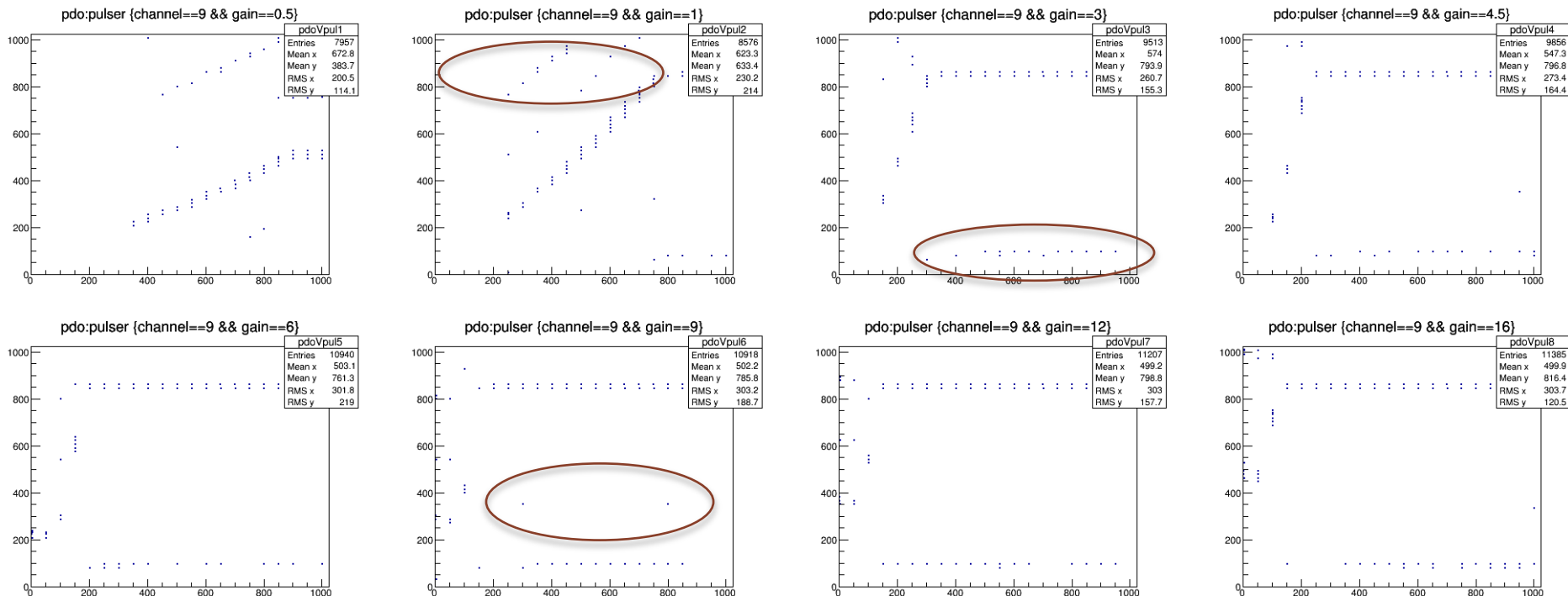
Development of Micro-Pattern Gas Detectors Technologies

- Micro Pattern Gas Detectors技術的發展とその応用を目指す。
- その技術の基礎と応用された研究に向けて必要とされる electronic-readout systemの開発も行なっている。
- APV25 , VMM prototypeを開発した。



Some bugs of VMM

しかし、VMM2 prototype チップにはバグがある。

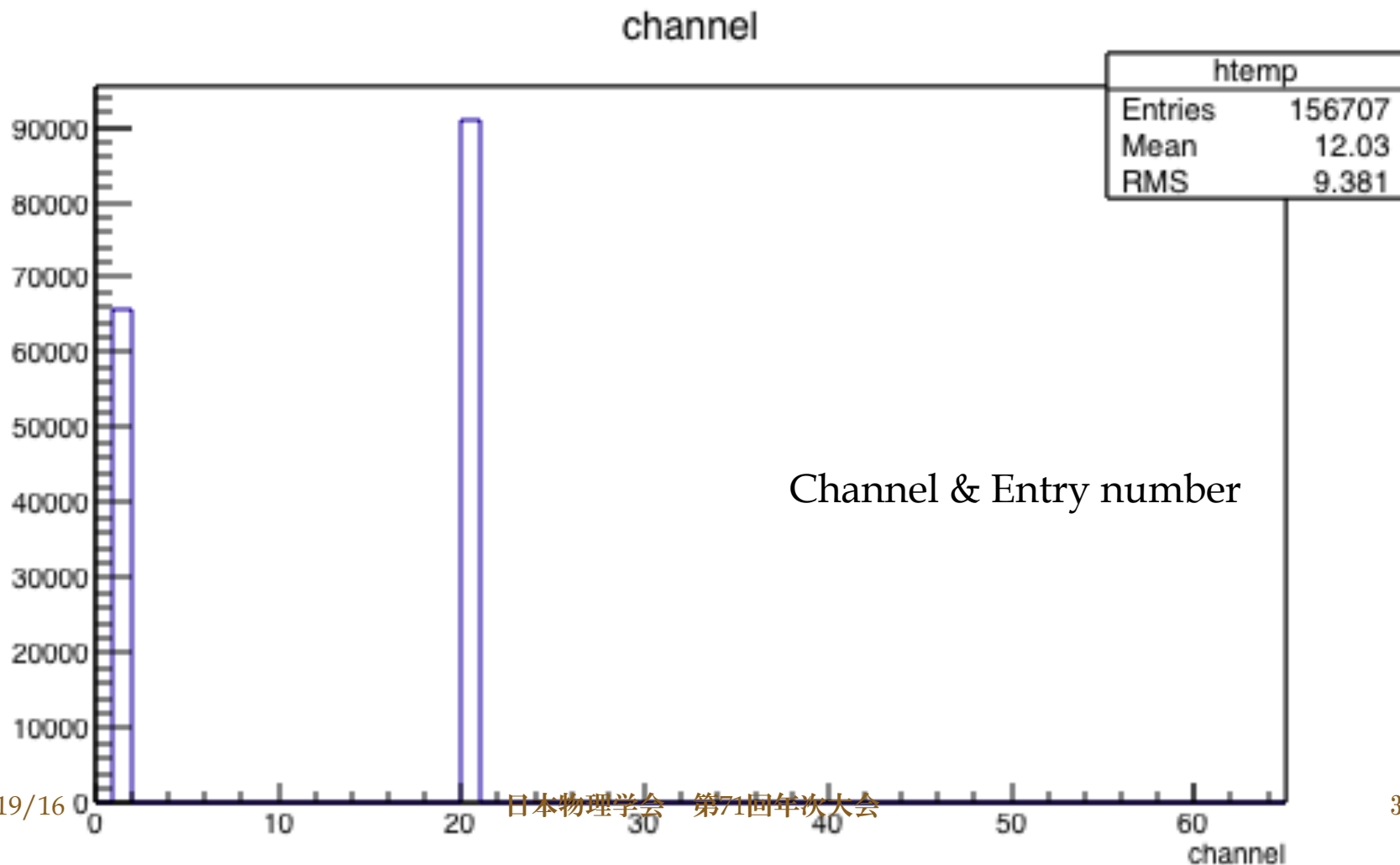


バグはどこからくるのか？

reason1) Cross talk reason2) bit flipping reason3) 原因が分からないバグ

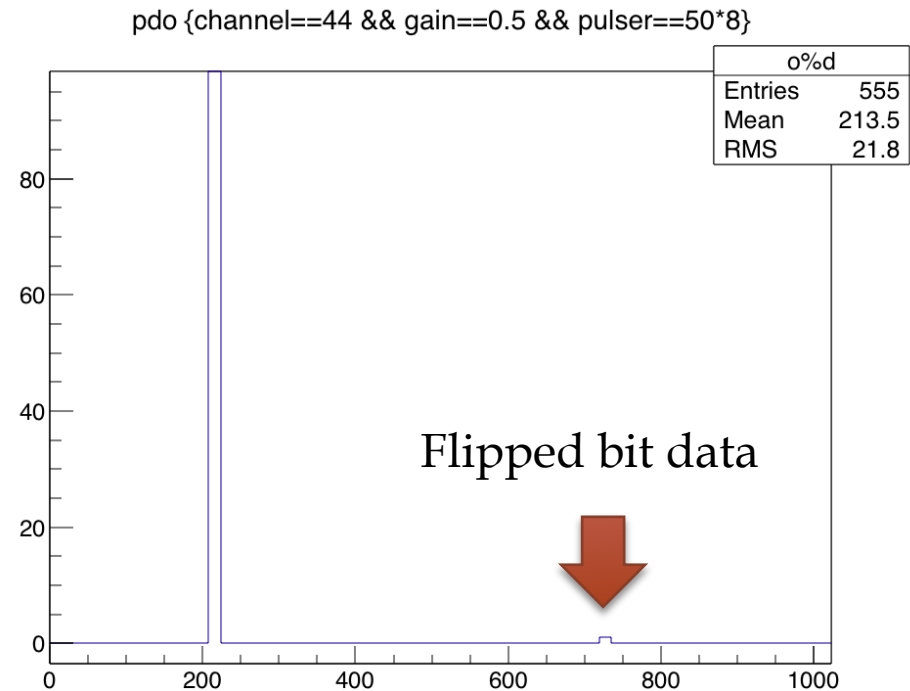
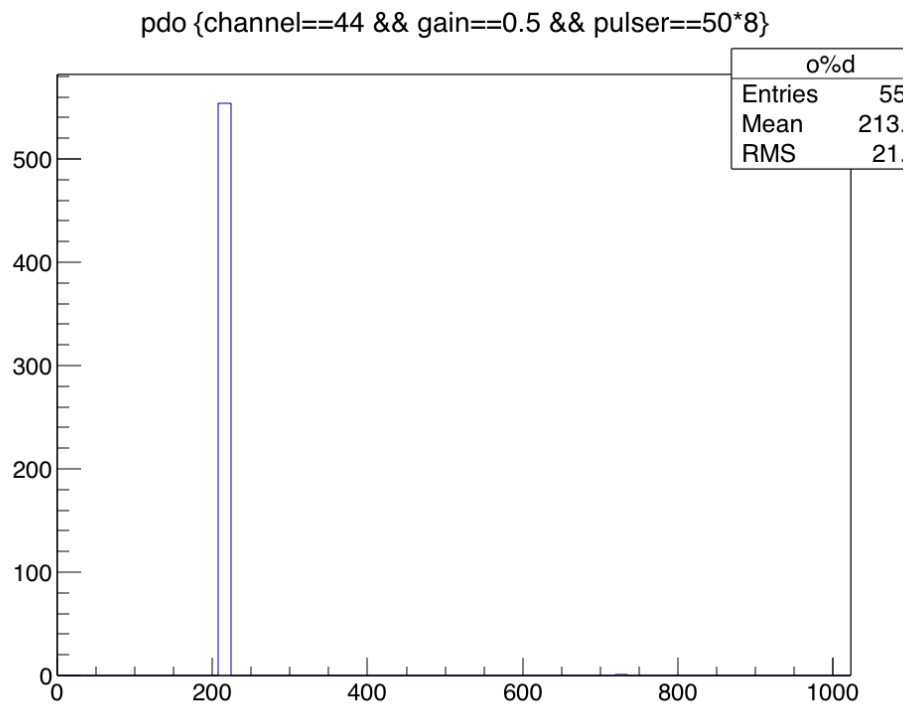
Reason 1) Cross talk (high gain and high Test Pulse DAC)

21チャンネルのみにアナログ信号を送った結果、違うチャンネルのでも反応をしていることが確認できた。



2) Bit flipping

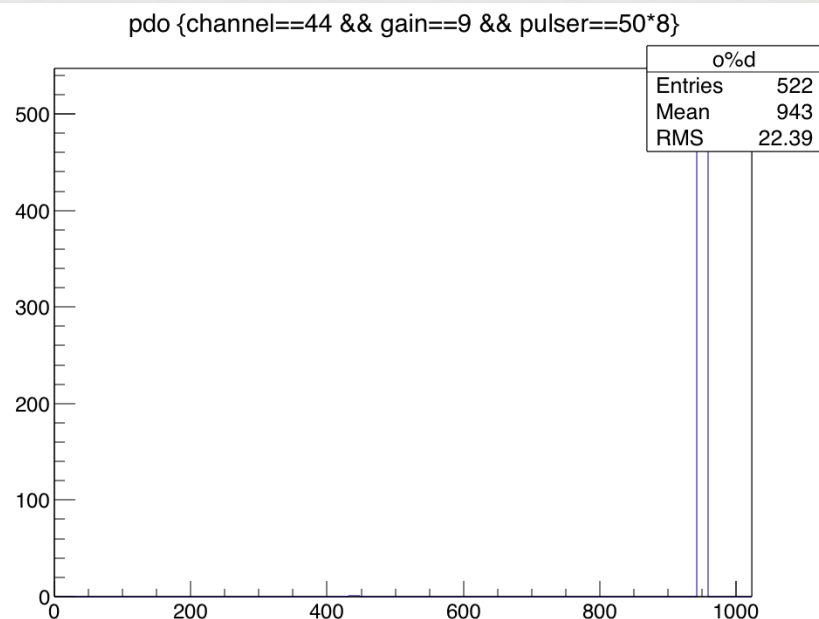
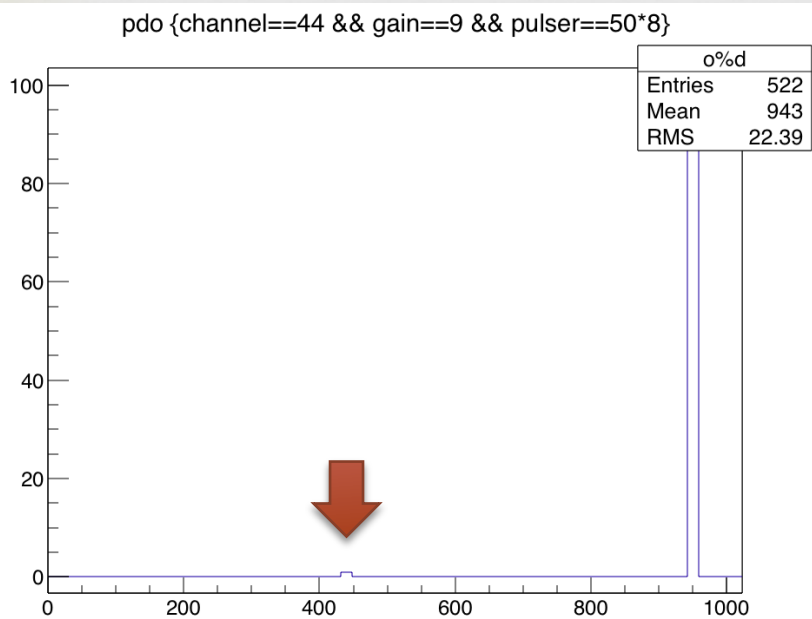
Meanデータの倍数に信号が来るように見える現象があった。



reason3) chip is bad.

Cross talkとBit flippingの現象以外にも原因が分からない

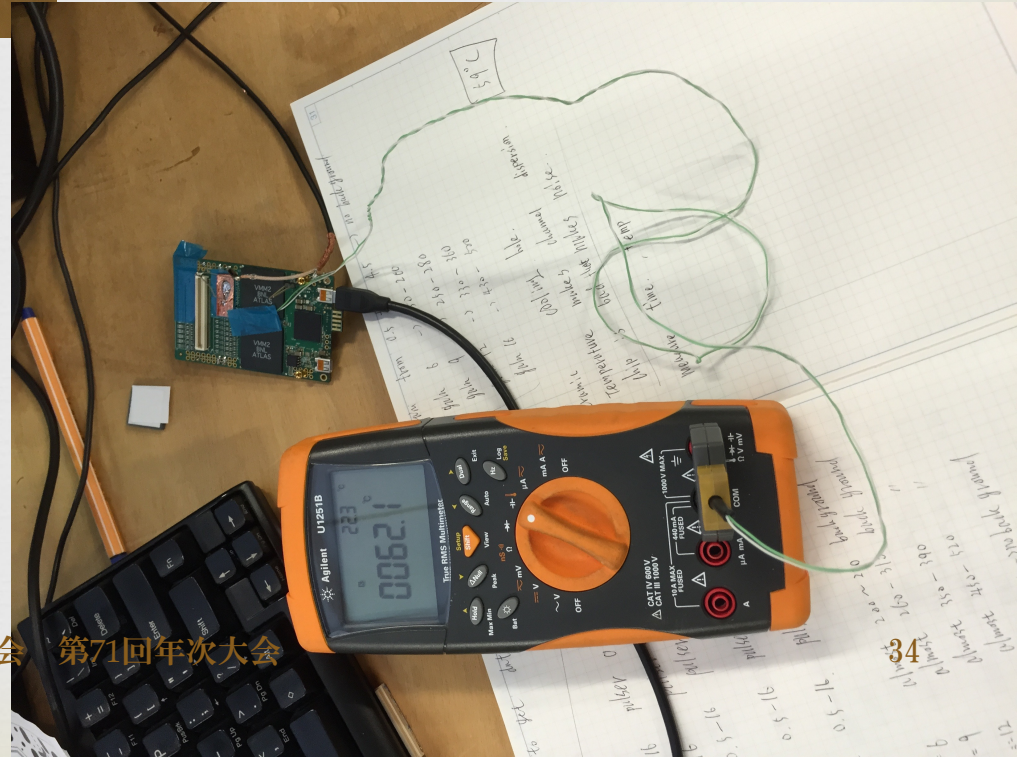
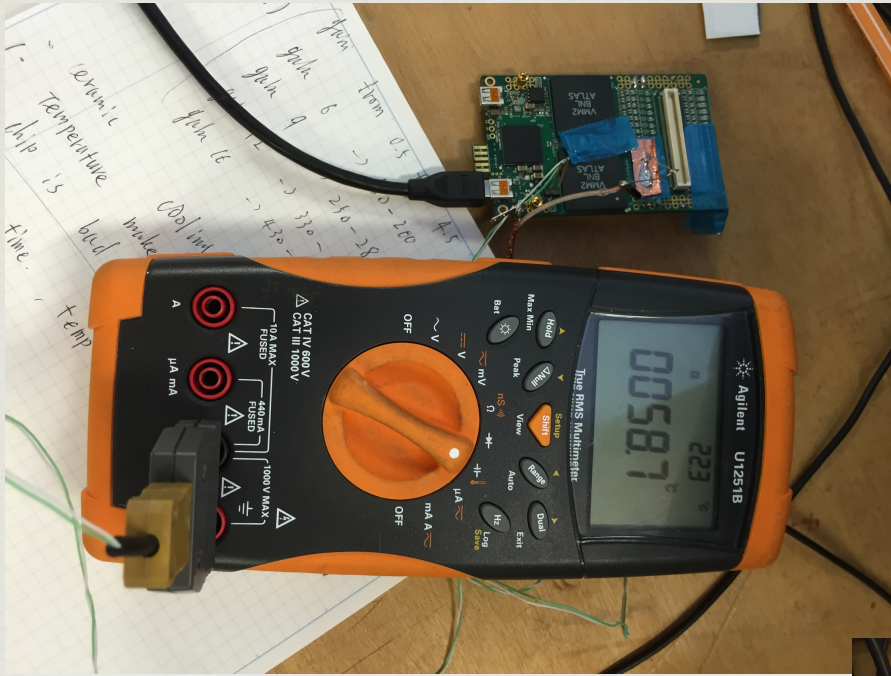
結果が見えた。この結果もprototypeのバグとして考えられる。



Check VMM2 Thermal data.

I tested thermal result of VMM2

With agilent u1251b.

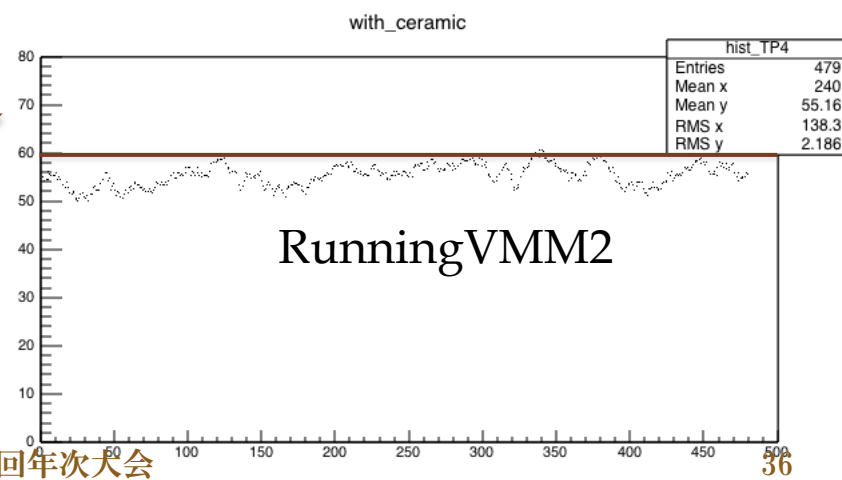
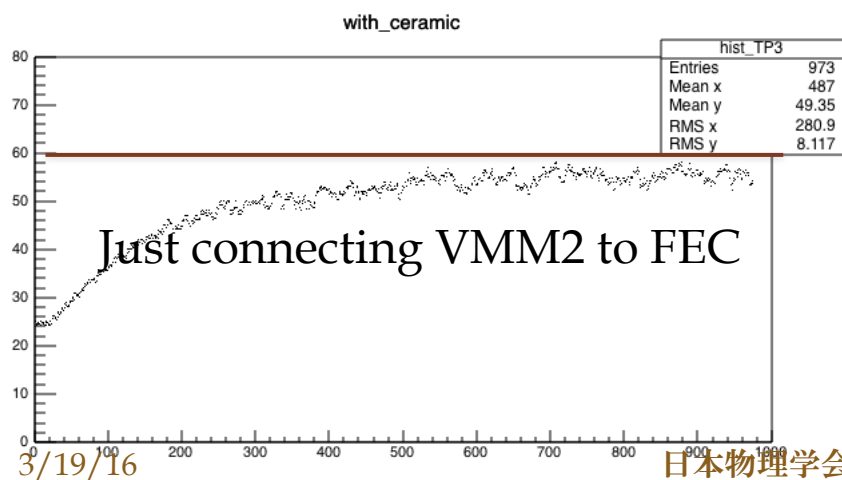
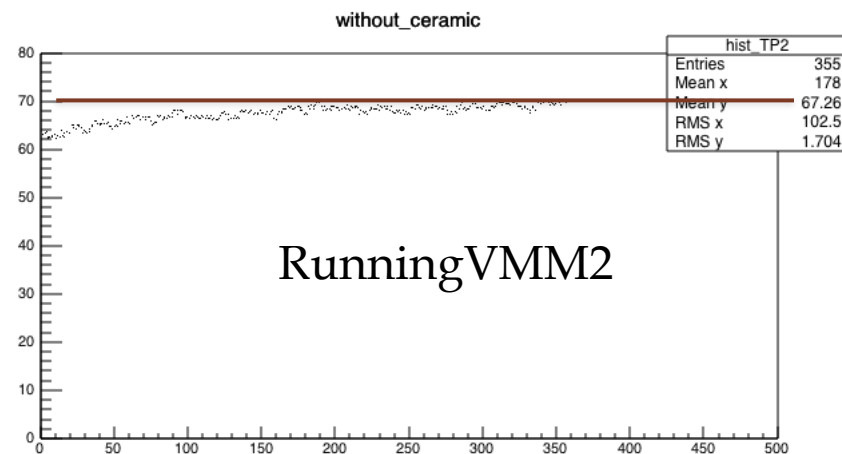
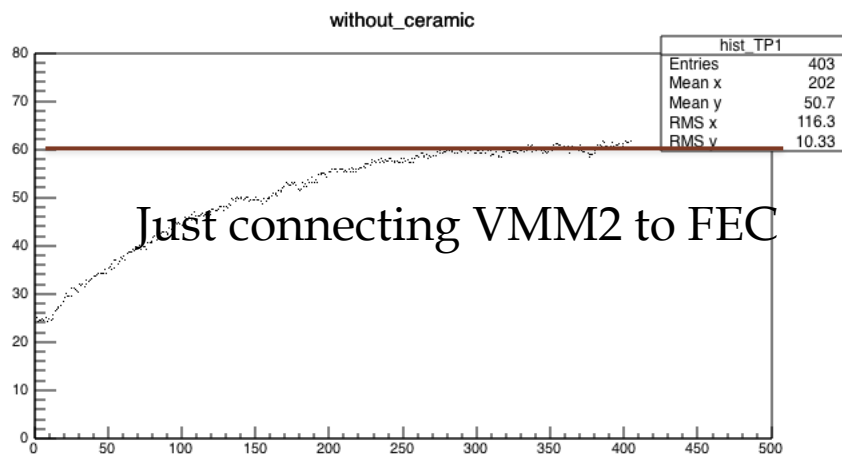


This Ceramic has
lots of small holes.

VMM2チップの温度が上がり、チップに損害を与える可能性があったため、
温度低下のため、Ceramicを用いたVMM2チップの温度調節

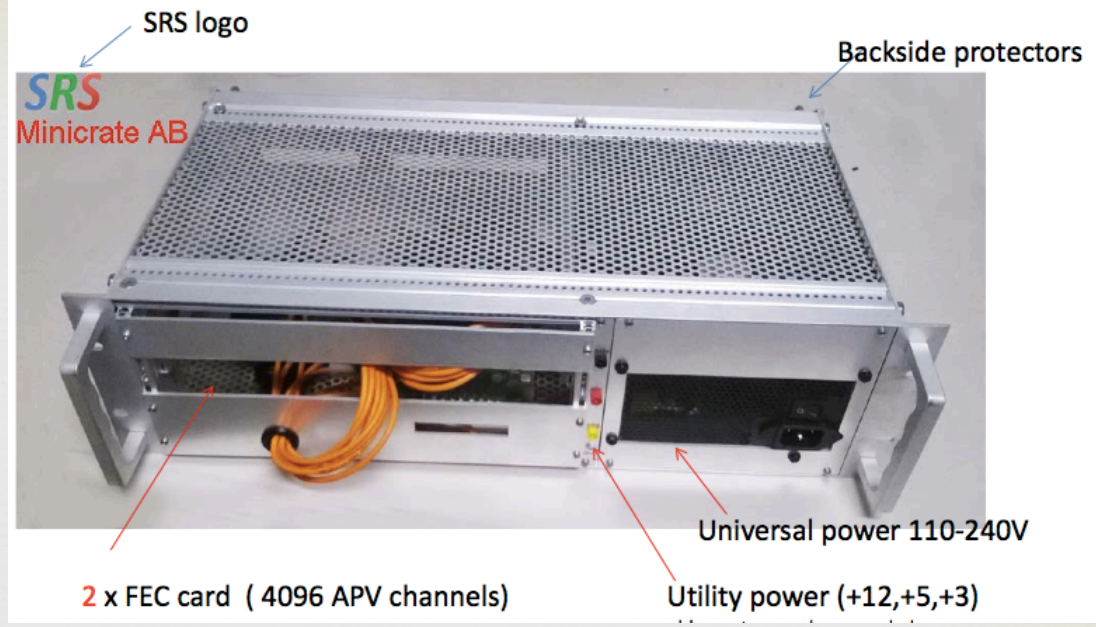
70°C->60°C

時間 Vs 温度

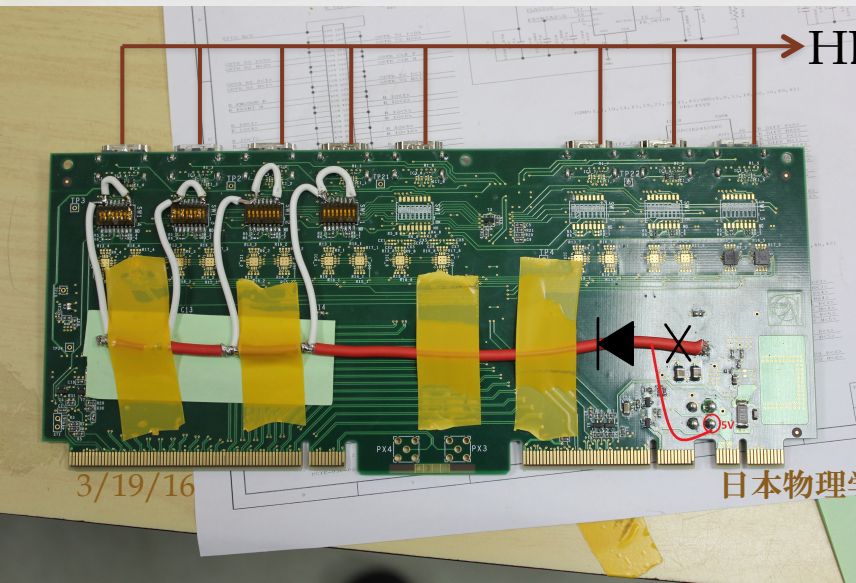


SRS System card

- D-CARD
<= VMM2から送られて来たデジタル信号をFEC boardに送る。
<= VMM2に電力を提供する。
(VMM2の消費電力はAPV25の3倍)
- FEC V6
<= D-CARDからのデータ进行处理し、PCへデータを送る。



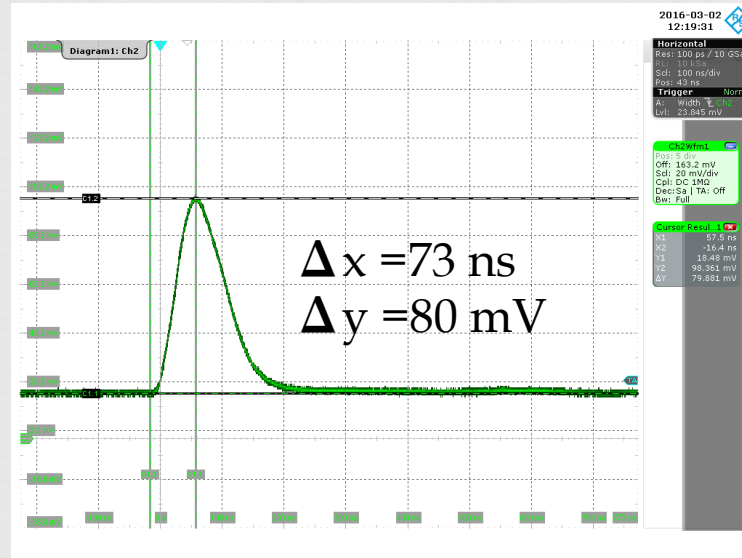
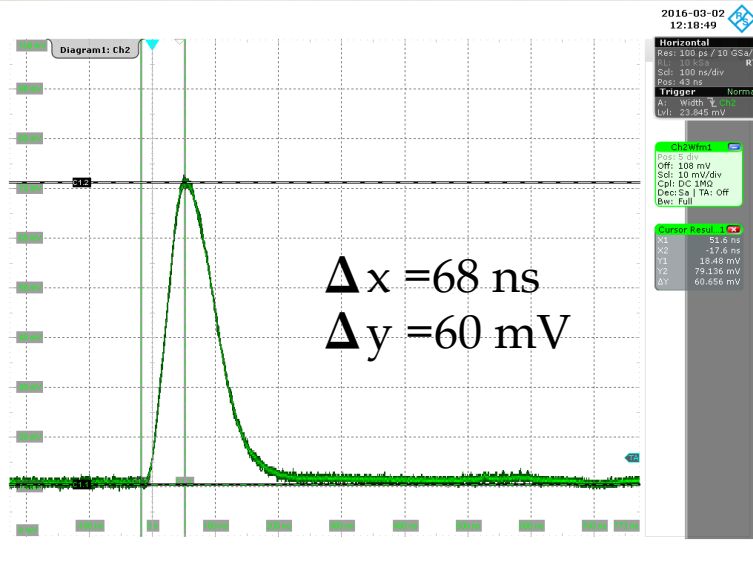
電源モジュールを搭載した mini crate などをまとめたシステムのことである
DCARD FEC V6



Analog response with internal pulser

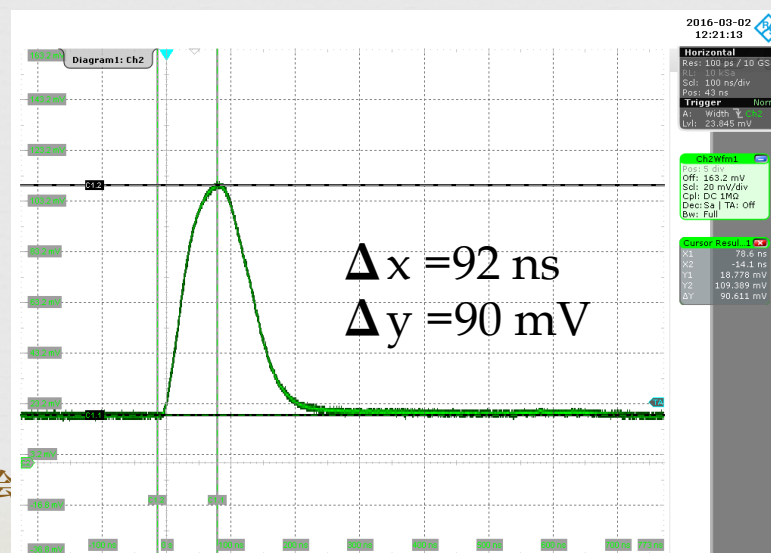
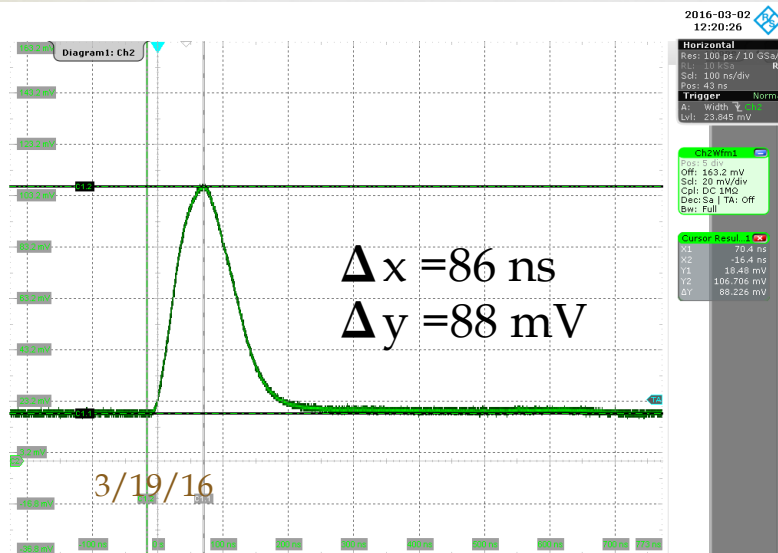
200

250

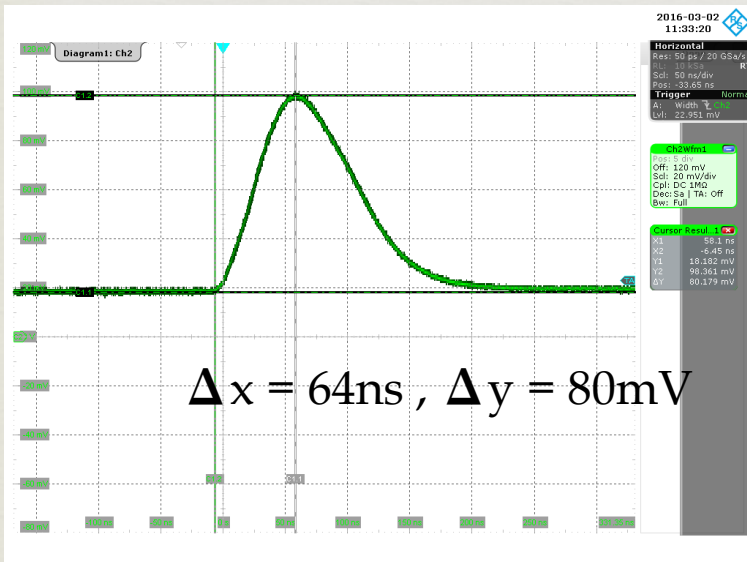


300

350

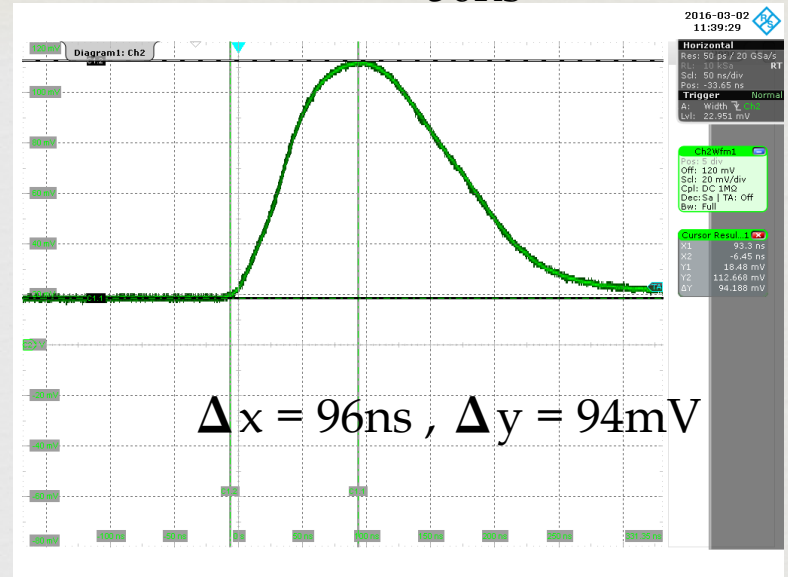


25ns



$$\Delta x = 64\text{ns} , \Delta y = 80\text{mV}$$

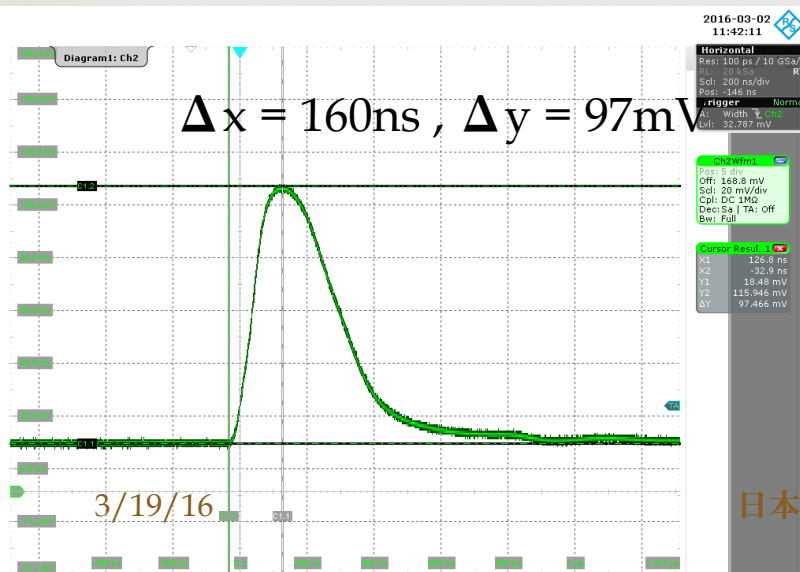
50ns



$$\Delta x = 96\text{ns} , \Delta y = 94\text{mV}$$

Gain 3.0 mV/fC , Test pulser DAC 400

100ns

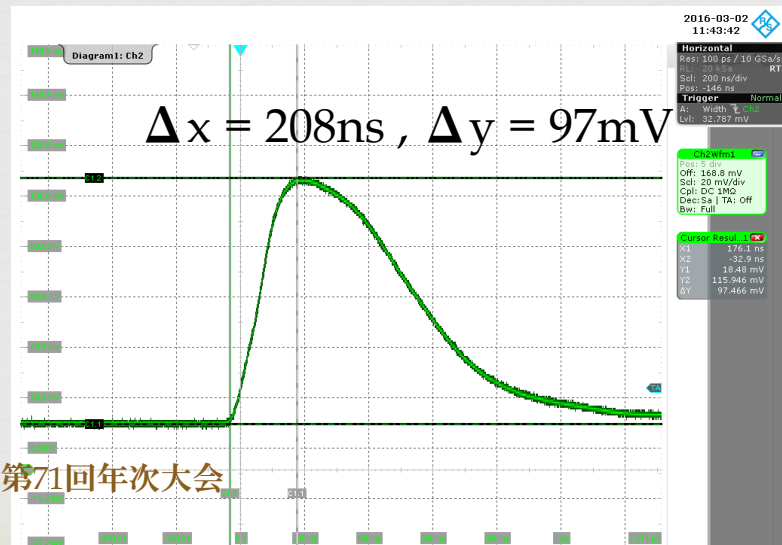


$$\Delta x = 160\text{ns} , \Delta y = 97\text{mV}$$

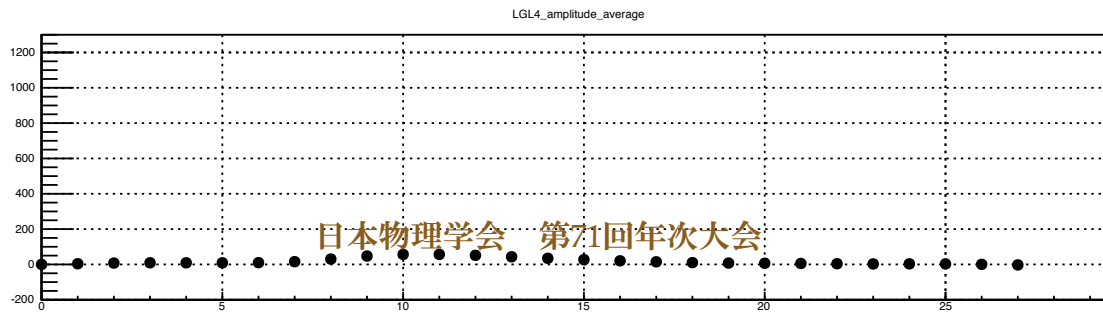
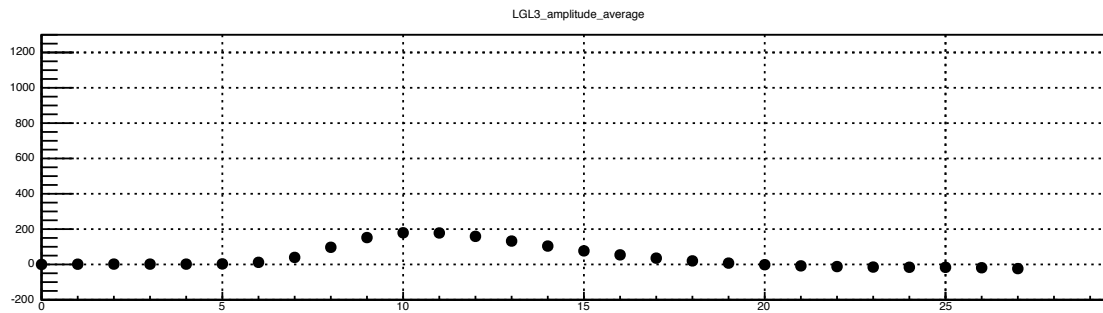
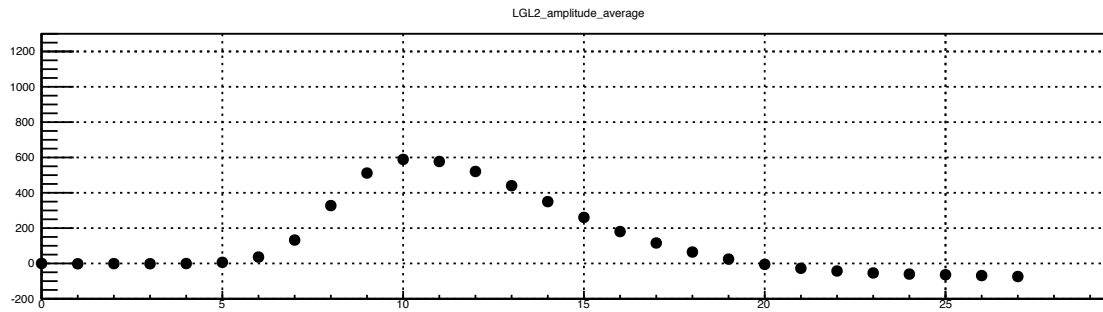
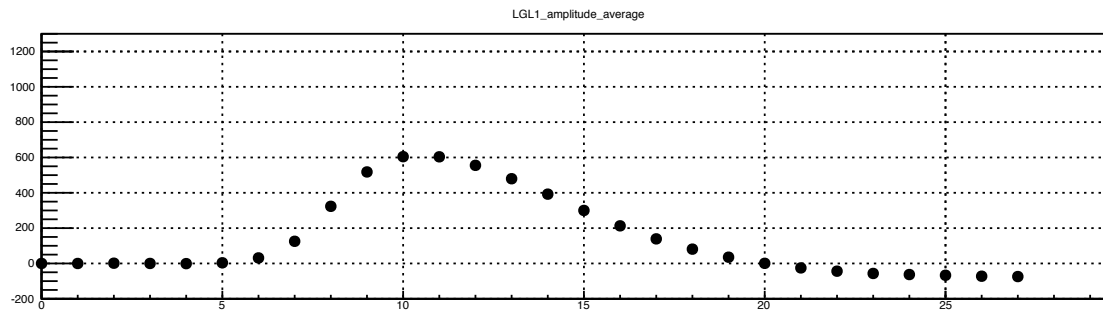
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200ns



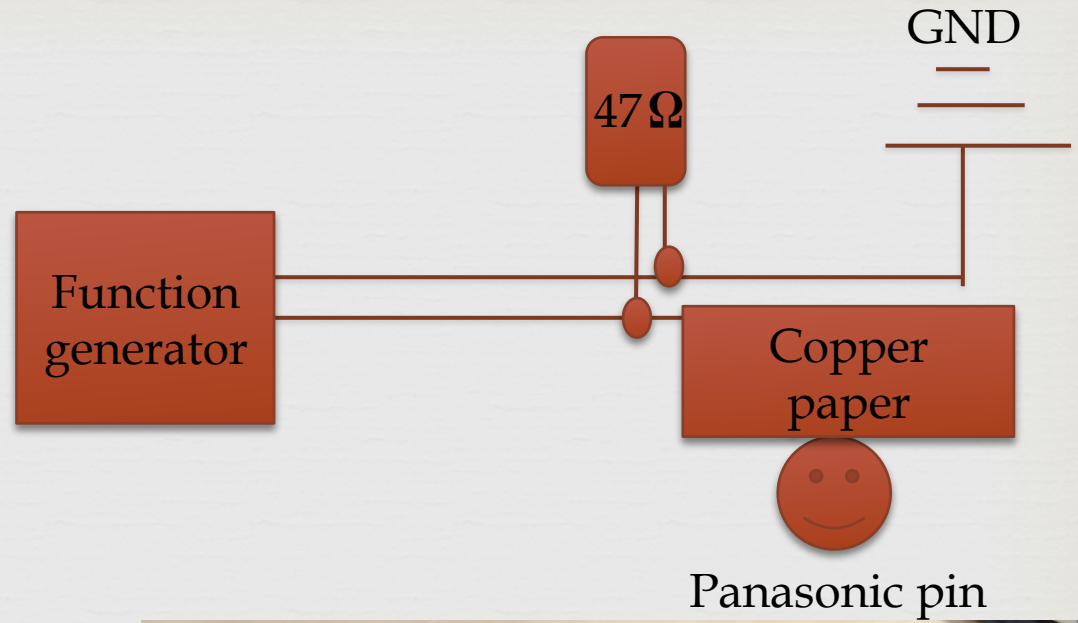
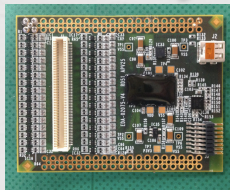
$$\Delta x = 208\text{ns} , \Delta y = 97\text{mV}$$





Nim Cable

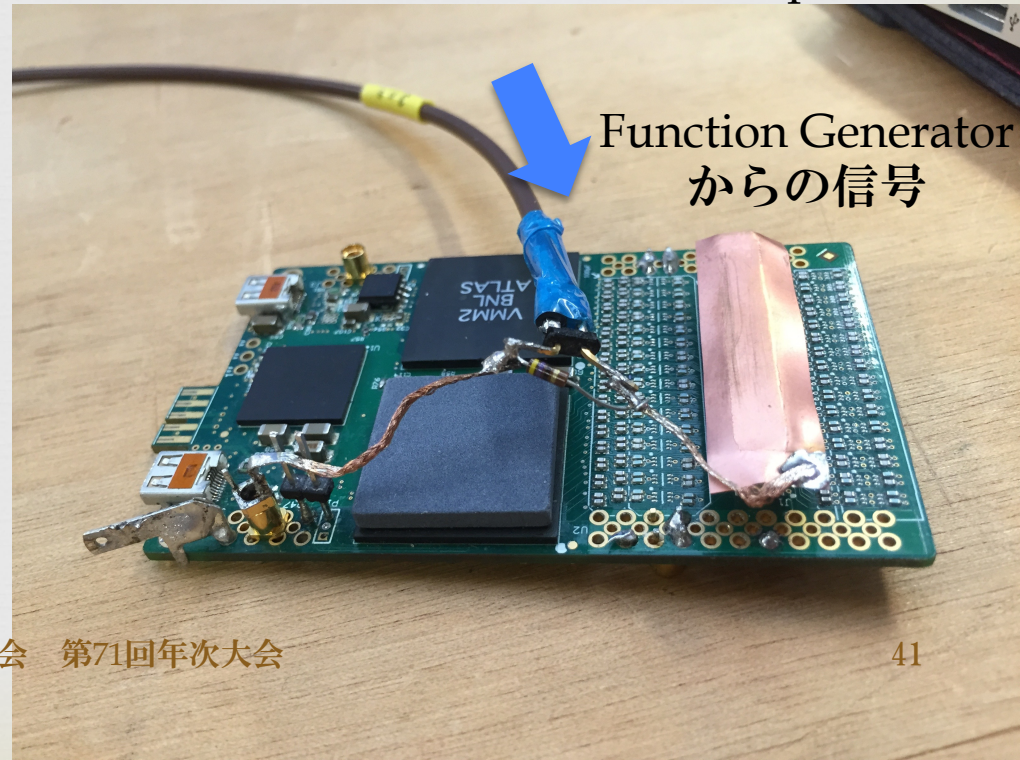
VMM2 chip



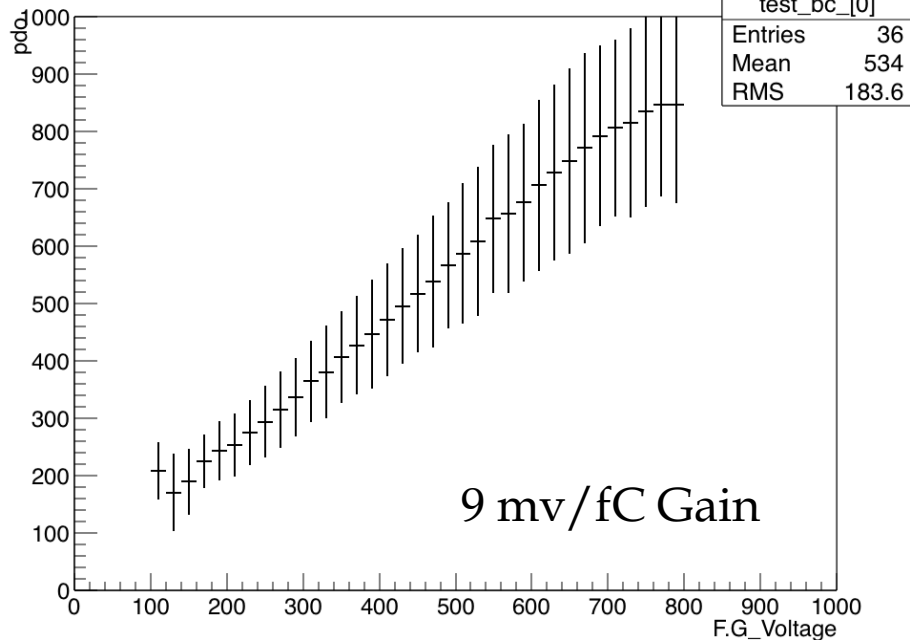
All channel test

128 ch pin + 2 GND pin

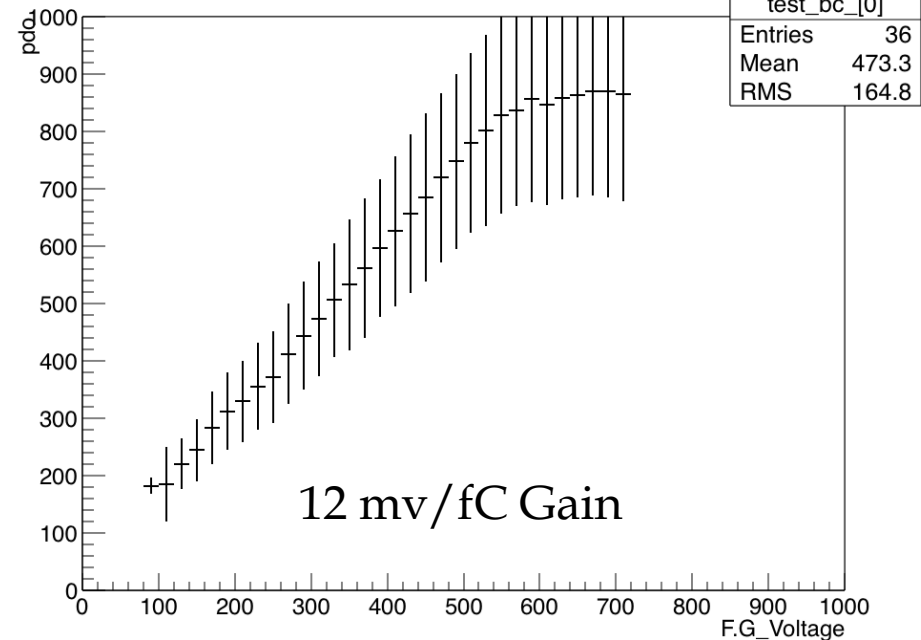
(130pin panasonic connector)



test_bc_[0]



test_bc_[0]



Data taking Condition

data trigger length 200ns
 delay time 0s
 trigger rate 2000Hz

F.G電圧 VS Pdo

結果

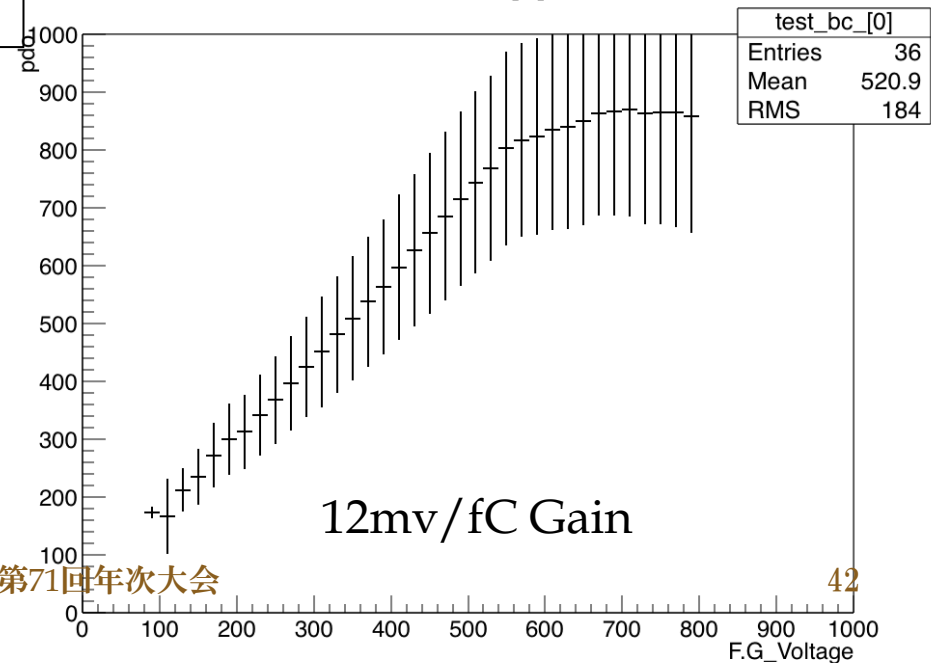
- 各チャンネル毎にPdo値が違う
- GNDの方にも一緒に信号を送って結果、データに揺らぎが生じた

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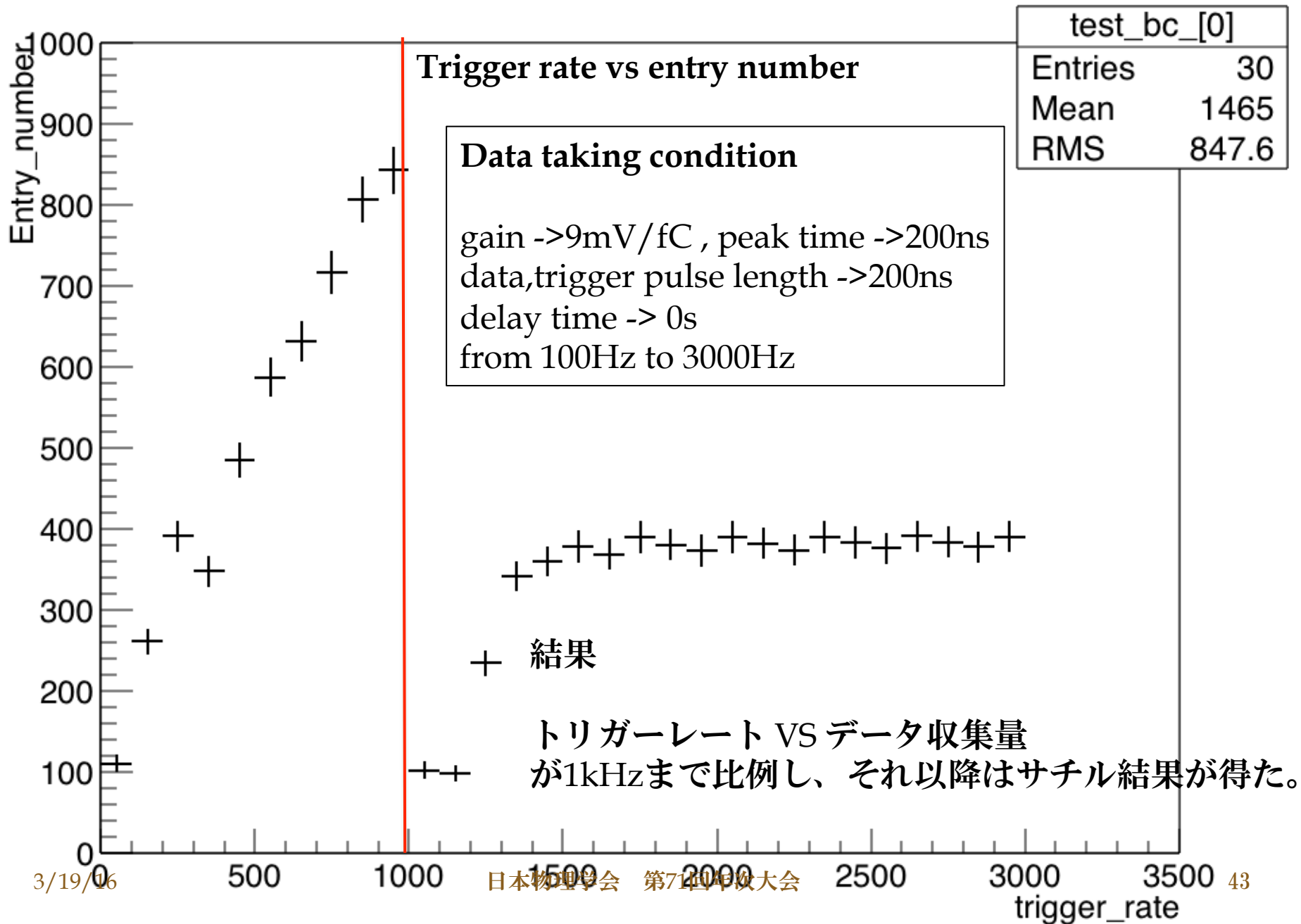
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test_bc_[0]



42

test_bc_[0]



External Signal test

Function Generator
External trigger & external signal



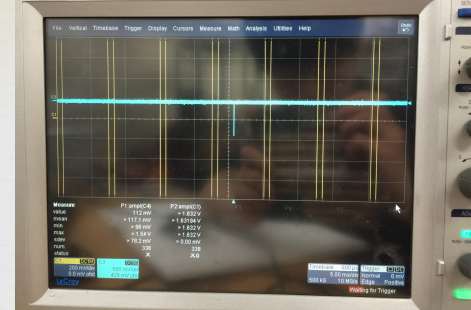
VMM2
Discriminator, shaper,
Peak & Time detector,
ADC(Analog Digital Converter)



SRS
D-CARD
+FEC(Front End Concentrator)



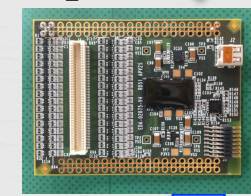
NTU Athens
Data taking & monitoring



Nim Cable

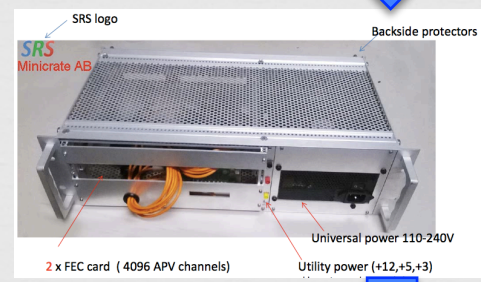


VMM2 chip



SRS

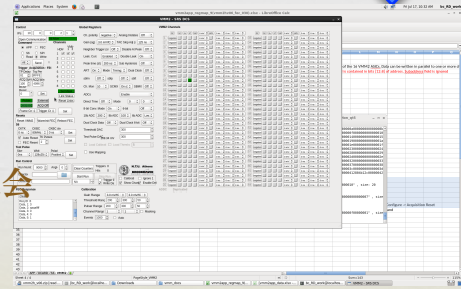
HDMI

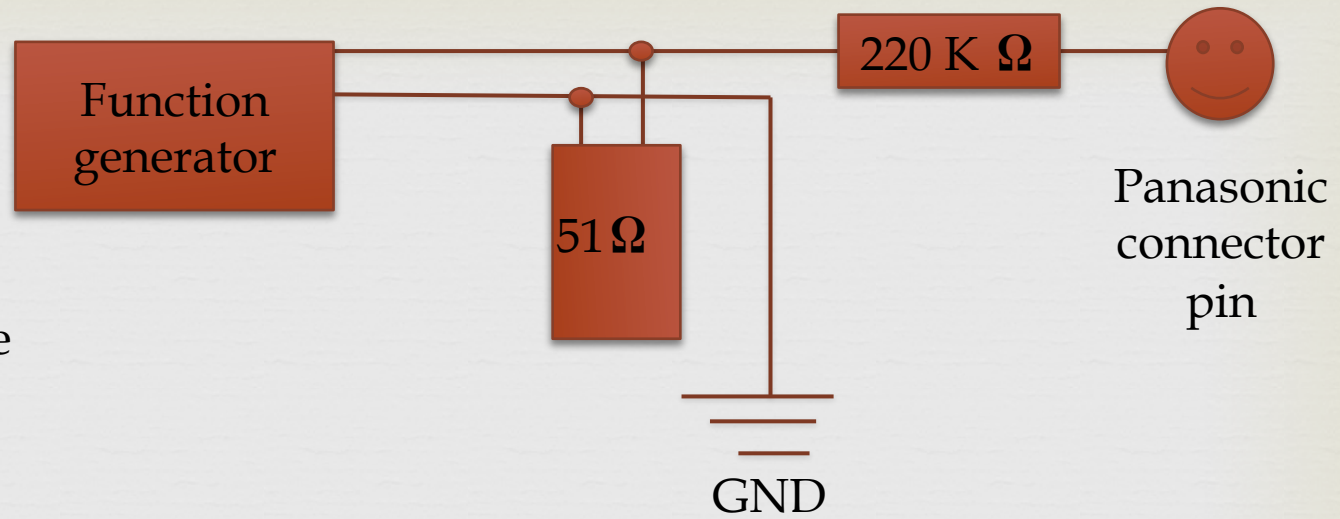


PC

Ethernet

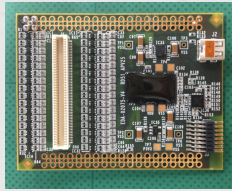
NTU Athens



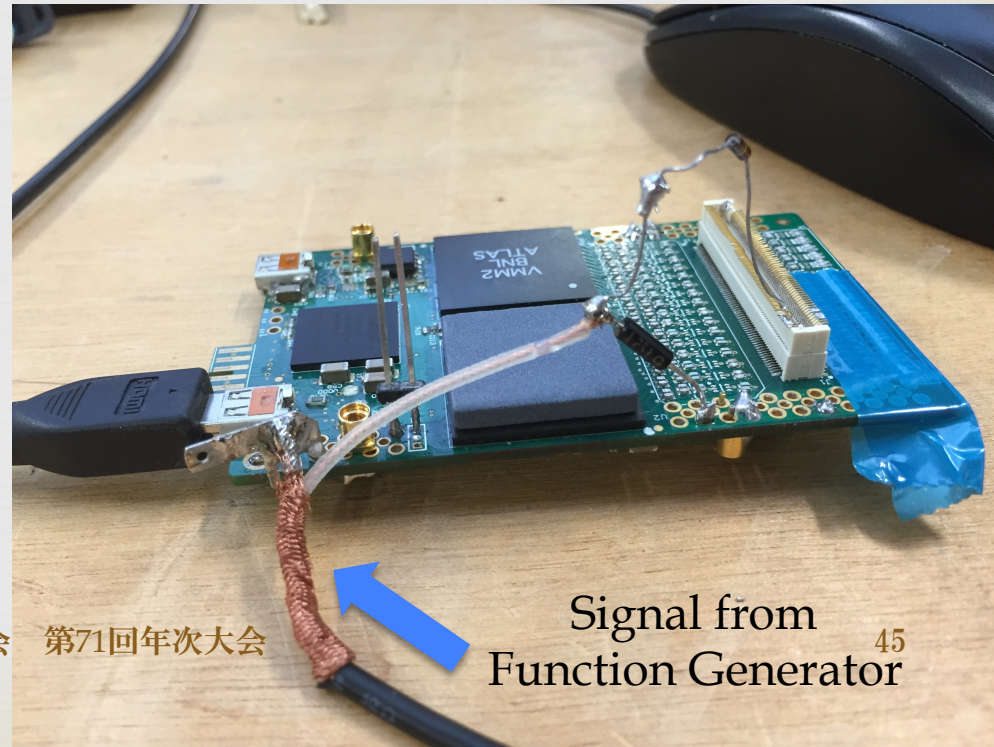


Nim Cable

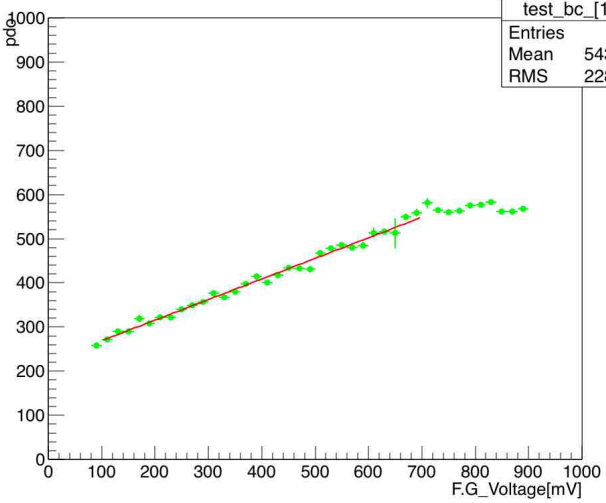
VMM2 chip



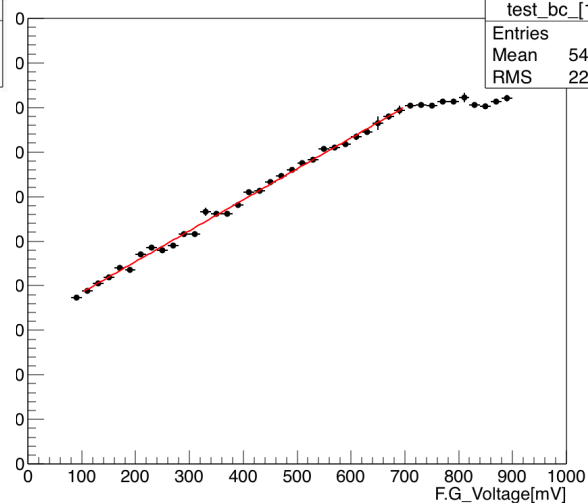
One channel test



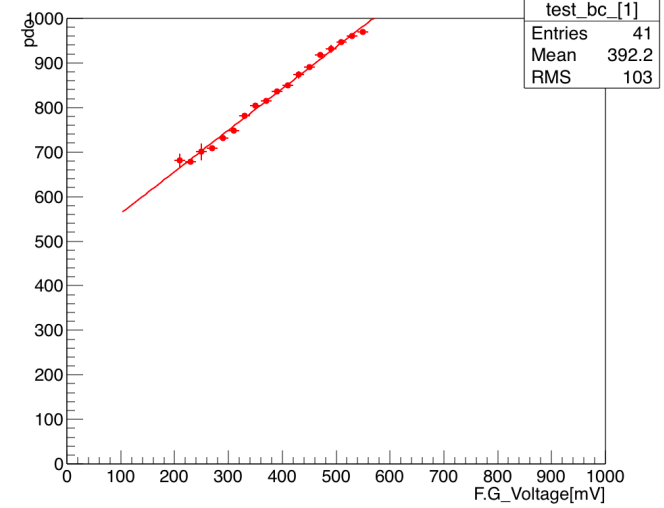
9.0mV/fC_gain



12mV/fC_gain



16mV/fC_gain



Channel 58

Peak time 200ns

lean_[0]

