MRPC-TOF R&D status

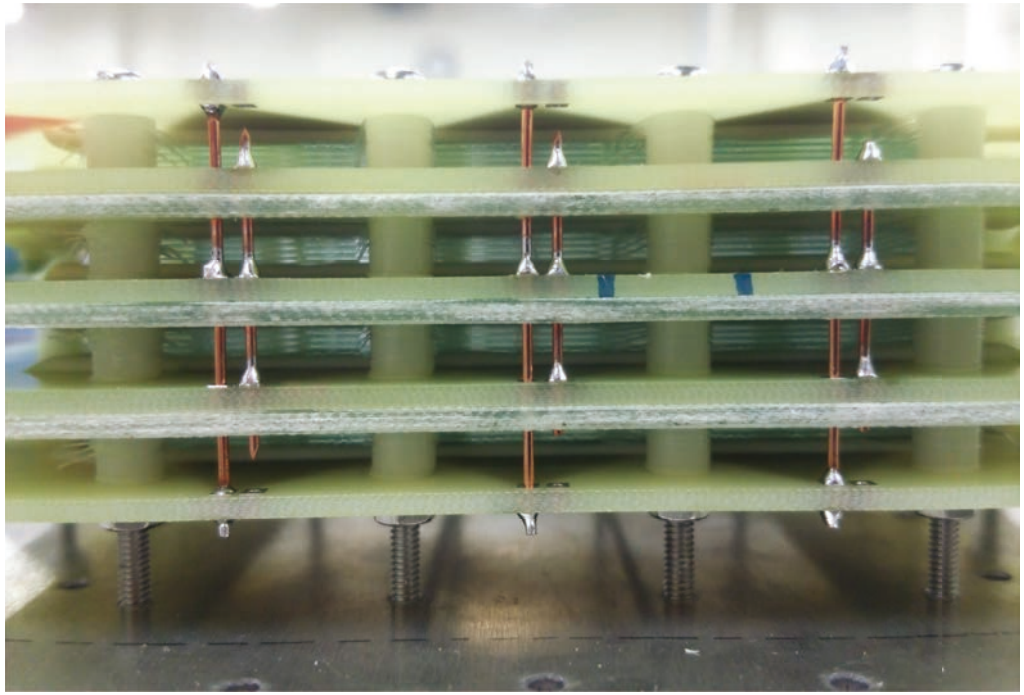
Tatsuya Chujo
(Univ. of Tsukuba)

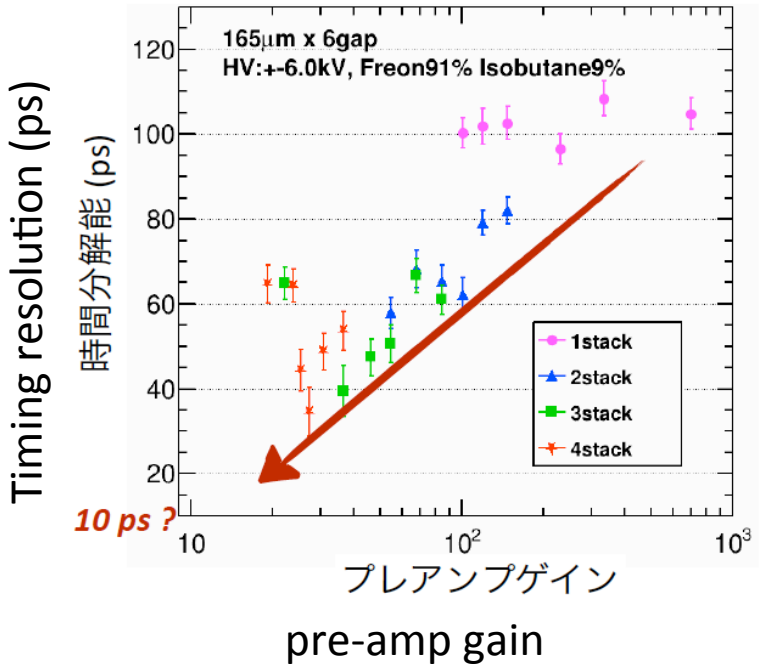
Members

- **University of Tsukuba:**
  - T. Chujo, T. Nonaka (D1), **K. Sato (B4) ***, R. Koyama(M1)
- **Tsukuba Technology University:**
  - M. Inaba
- **JAEA:**
  - H. Sako, S. Sato
- **KEK:**
  - K. Ozawa, K. Aoki

* Graduation thesis in 2016, presentation at JPS2016 spring (poster session for undergraduate students)

4 stacks MRPC in Tsukuba (2014-)



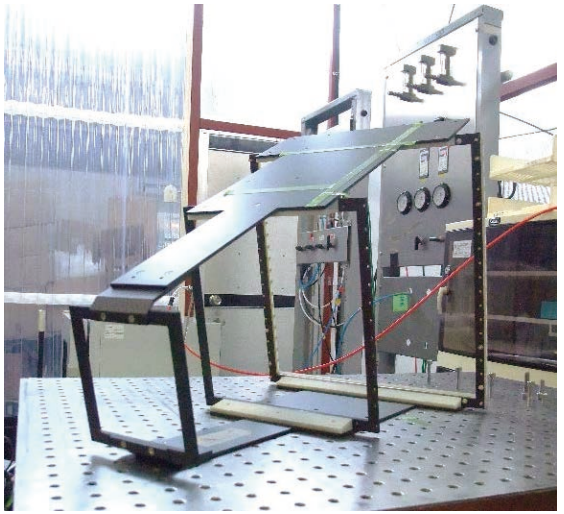


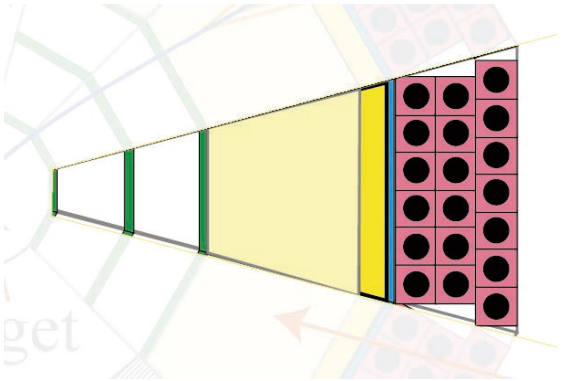
4 stacks MRPC (6 gaps x 4)
T. Nonaka (U. Tsukuba, 2015, master thesis)

Approaching to 30 ps timing resolution.
Current best & reliable value of timing resolution of this type of MRPC: 47.5 ps (cosmic ray)

MRPC-TOF in E-16

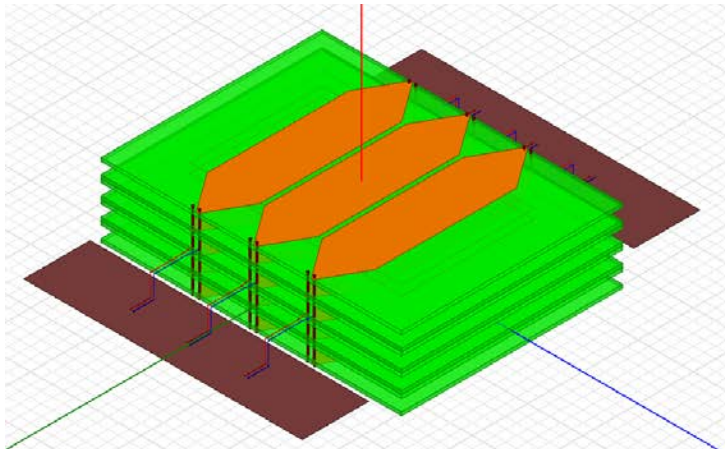
- **MRPC-TOF meeting, June 18 & September 2, 2015 @ Univ. of Tsukuba**
  - Discussed a plan of E-16, and possibility to install a new MRPC-TOF in E-16
  - It is possible to install MRPC-TOF in front of PbGl, behind HBD. Coverage will be around 60 x 60 cm^2 per segment, 4 segments at forward direction.The available gap space between HBD and PbGl will be ~ 5cm.
  - Flight path will be 1.2 m.
  - E-16 schedule: 2017 fall, physics run start.
  - Start conter (diamond beam counter?)
  - ELPH test beam in Feb. 2016 (postponed to May 2016)





Collaboration with SONY

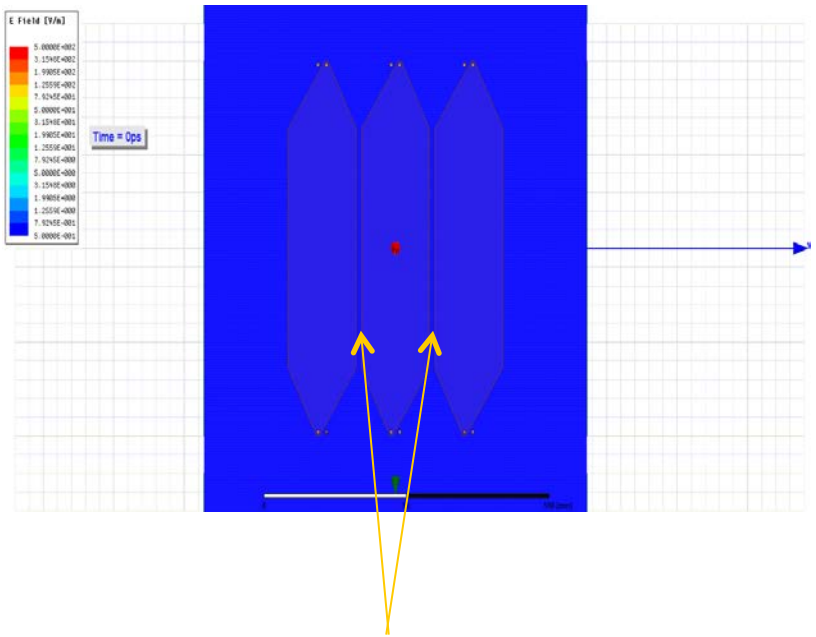
- ソニーイーエムシーエス株式会社
  設計技術部門　電気CAE技術部
  - Modeling MRPC detector
  - Electromagnetic field cal. by solving Maxwell eq. numerically.
  - Consulting of fast signal propagation in electrodes, cables, impedance matching, and actual test.



An example: proposed modifications (SONY)

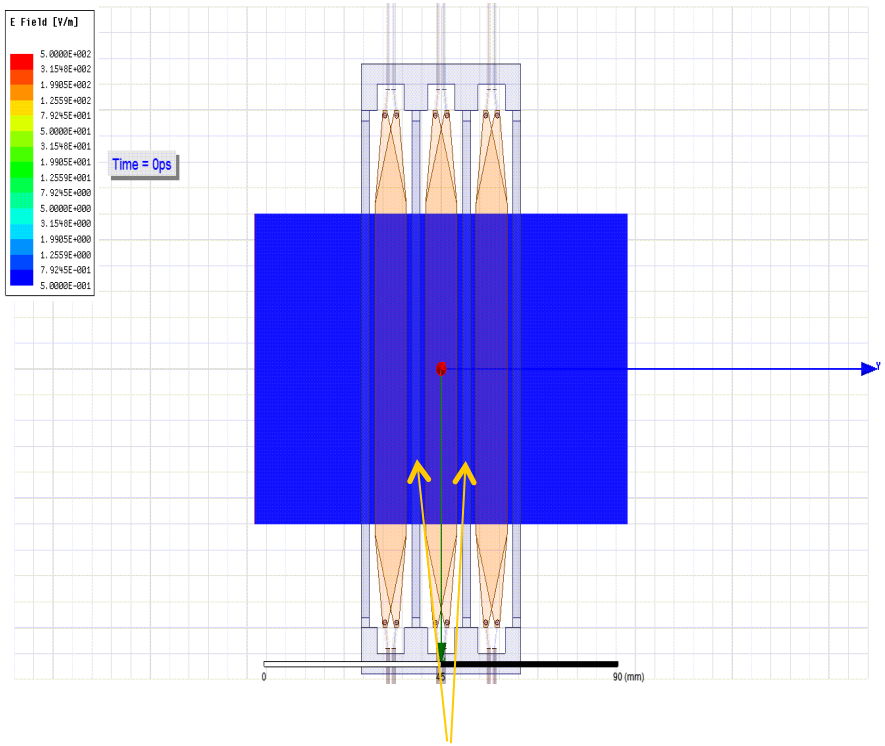
Electric filed near electrodes（as a function of time）

Default



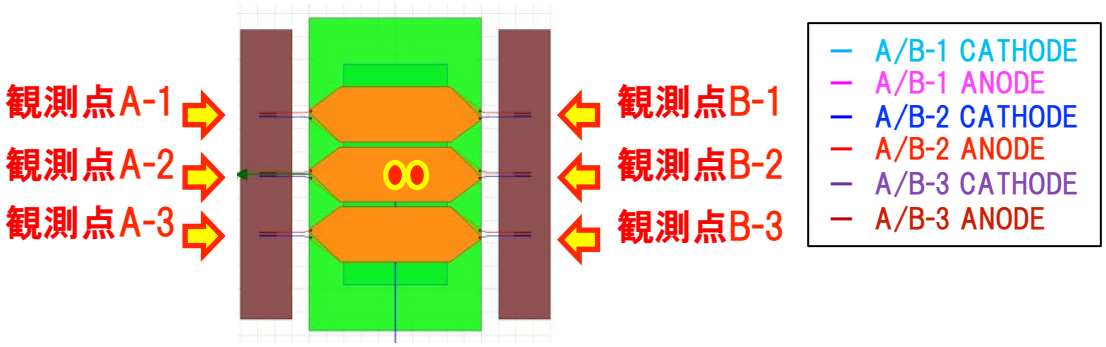
high density of electric field on the edges of electrodes
⇒interference

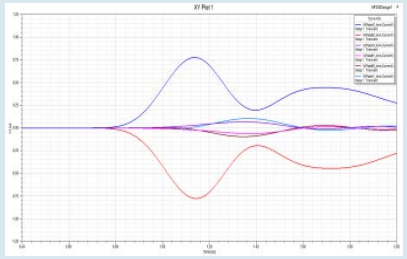
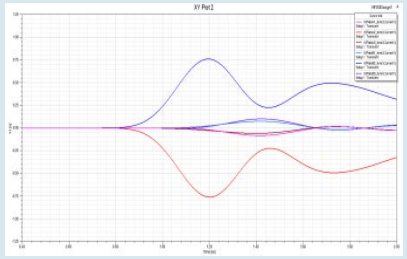
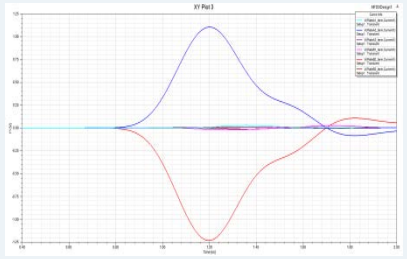
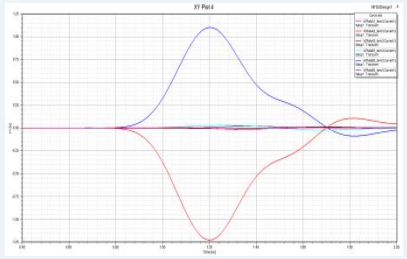
Modified (Ref. conductor)



Ref conductor, reduce the dispersion of electric filed⇒small interference

Example: Pulse response



	A側	B側
Default		
改善提案①		

Merit

- Lager amplitude
- Reduction of reflection
- Reduction of interference between adjacent electrondes

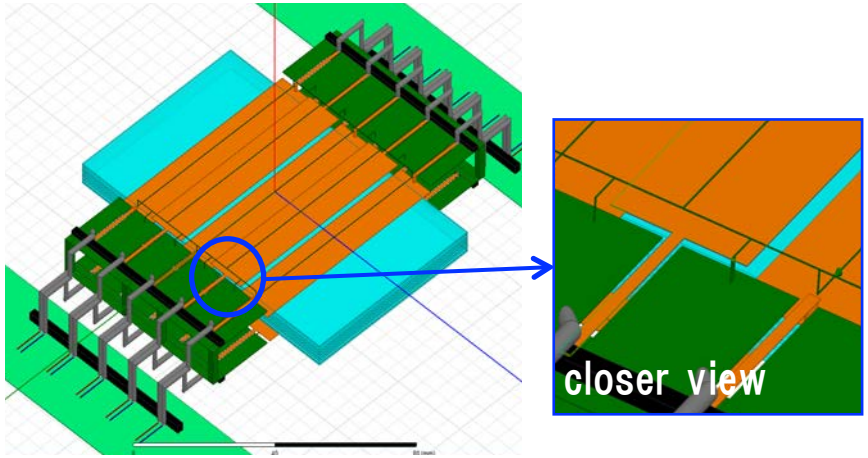
Demerit

- Reduce electrode area
  ※ width 24mm⇒8mm
  ➔ reduction of efficiency.

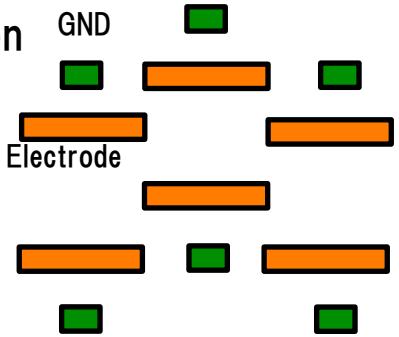
Proposed modification（Dec. 2015）

Plan ①: Multi layer PCB

- Electrodes in the different layer of PCB
- GND above electrodes
- Add current on near-by electrodes (by a different circuit)

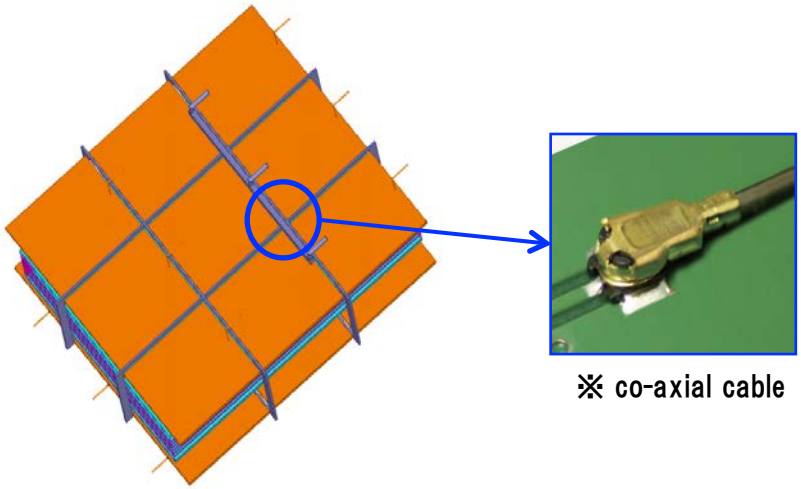


cross section (image)



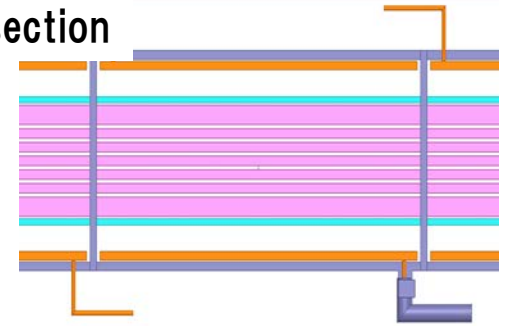
Plan ②: Patch structure

- electrode pad: 24mm×24mm
- put co-axial connector and cables on each pad



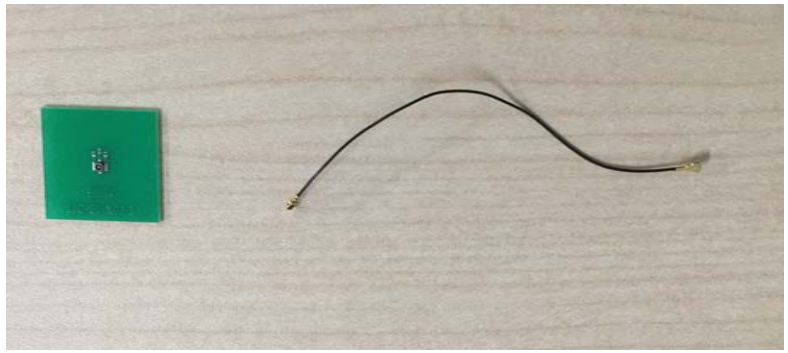
※ co-axial cable

cross section



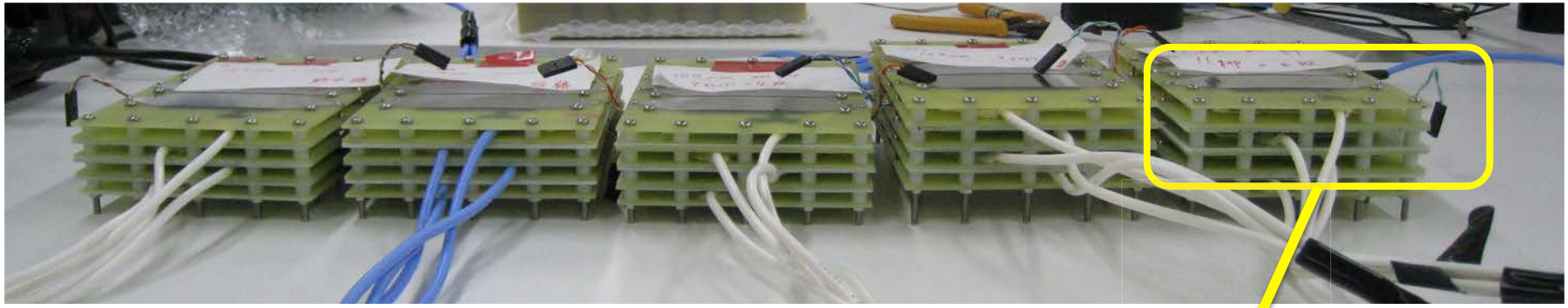
Future Plan (SONY)

- Continue R&D with SONY, and test with actual detectors by building new proposed designs in 2016.
- R&D key points:
  - Grounding, signal reflection, impedance matching, preamp design.
  - build prototype will be tested at ELPH beam test in May, together with the planed MRPC prototypes.

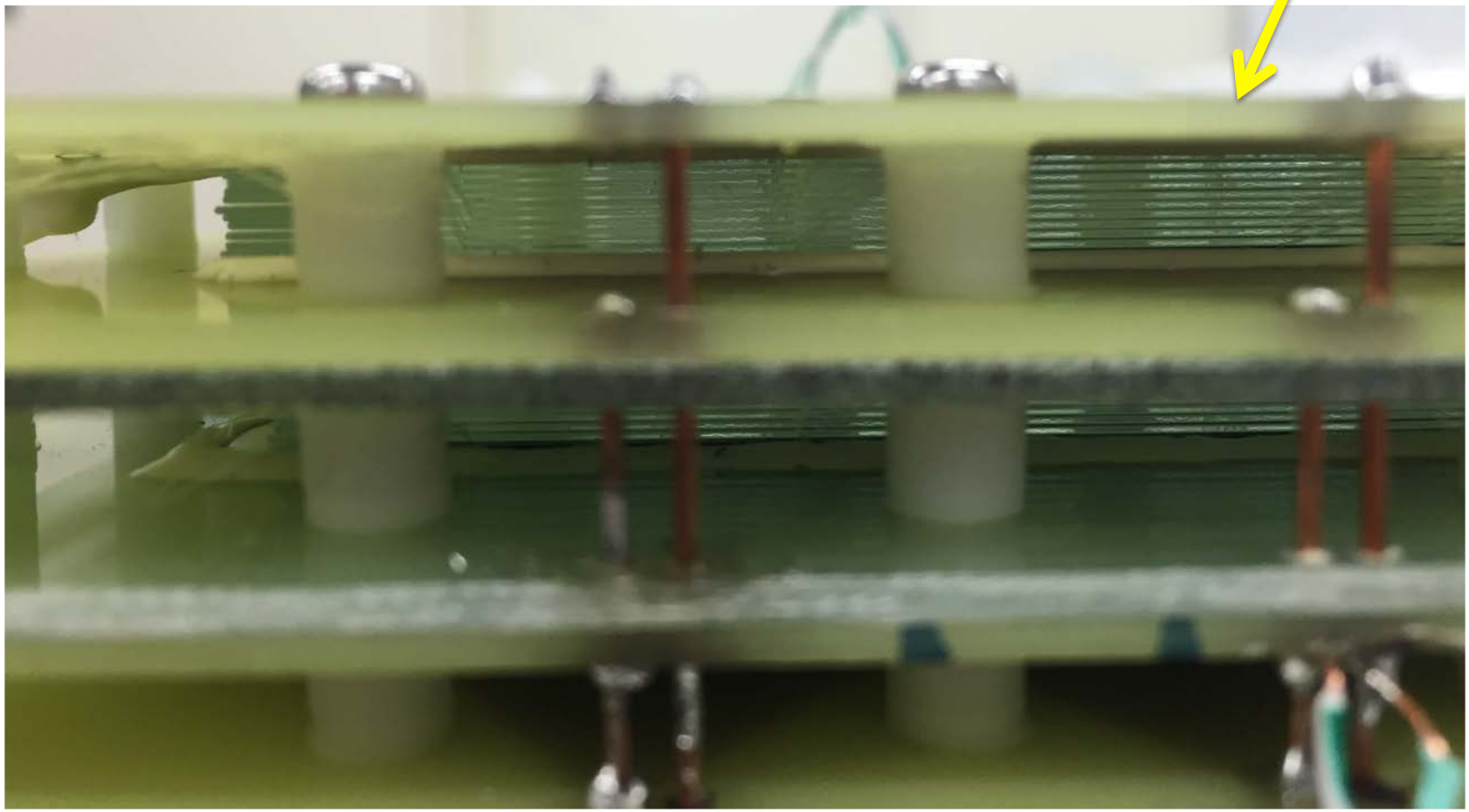


New 4 stack prototypes in Tsukuba for ELPH test beam (K. Sato, R. Koyama, T. Nonaka)

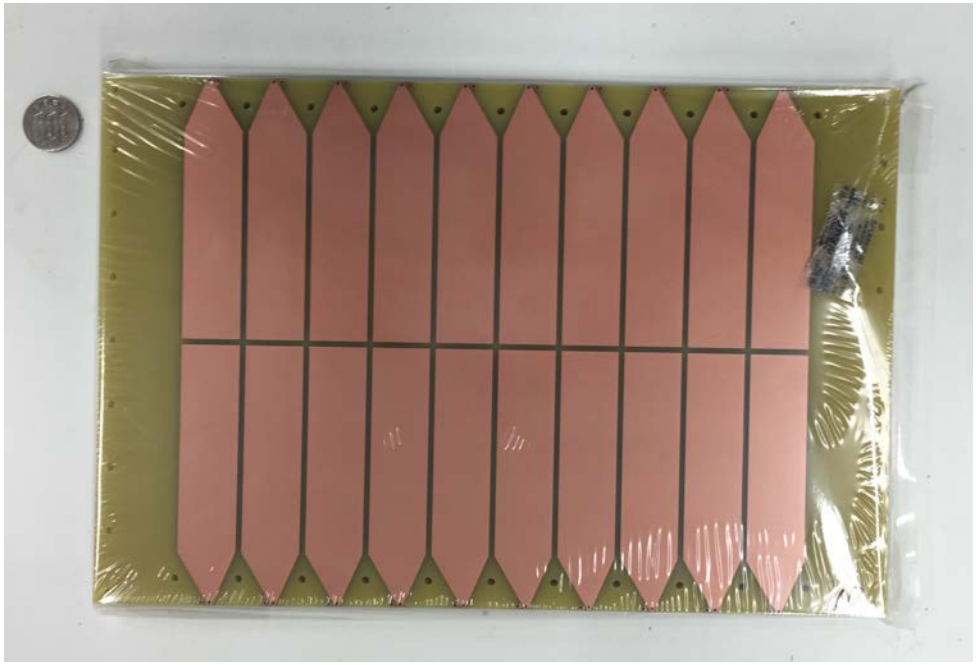
165 micron, 6 gaps (default)	148 micron, 6 gaps	128 micron, 7 gaps	104 micron, 9 gaps	90 micron, 11 gaps

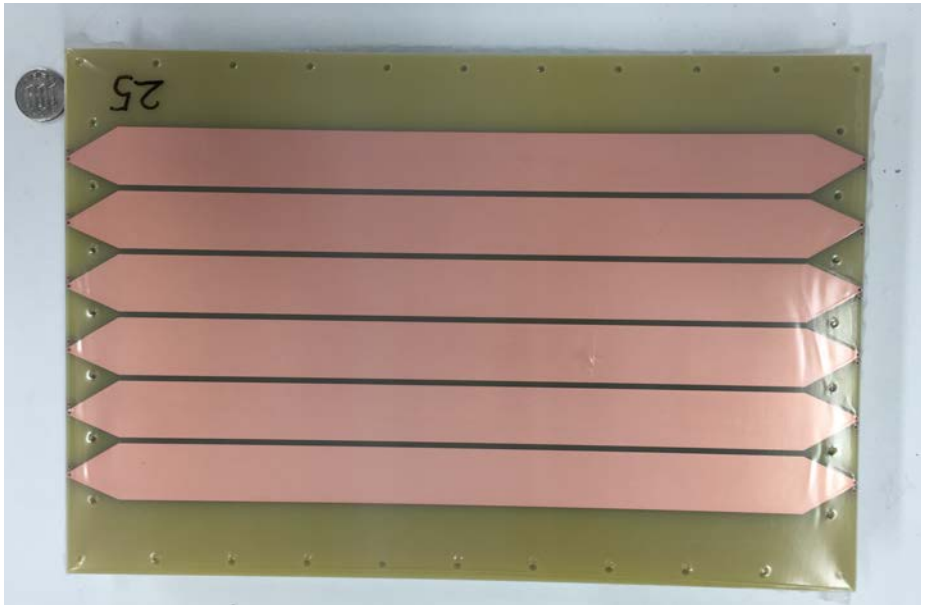


90 micron,
11 gaps



Medium area MRPC prototypes





- Two types (pad and slat) PCB have been made.
- 20 cm x 30 cm PCB size
- To be build lager size 4 stack MRPCs and tested at ELPH.
- It could be a prototype for E-16.

Summary & plan

- Build several types of MRPC for ELPH test beam.
- Currently tested at cosmic ray at the test bench, Univ. of Tsukuba (K. Sato).
- Started the collaboration with SONY (signal propagation and design, etc.)

- Plan in 2016:
  - ELPH test beam in May, 2016.
  - Further R&D with SONY and M. Chiu (BNL)
  - Readout R&D using DRS4, and prototyping.
  - Final design of MRPC for E-16.